The Thesis Committee for David Carl Dillen
Certifies that this is the approved version of the following thesis:

Confined Electron Systems in Si-Ge Nanowire Heterostructures

APPROVED BY
SUPERVISING COMMITTEE:

Supervisor:

Emanuel Tutuc

Sanjay K. Banerjee

Confined Electron Systems in Si-Ge Nanowire Heterostructures

by

David Carl Dillen, B.S.

Thesis

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Master of Science in Engineering

The University of Texas at Austin

August 2011

Acknowledgements

I would like to thank all those who have helped me along the way to writing this thesis, making the process easier and more enjoyable.

First, and foremost, I want to express my appreciation to my advisor, Dr. Emanuel Tutuc. His constant guidance and thoughtful critiques of my work have helped me immensely. These qualities, combined with his extensive knowledge of physics and engineering, have made me a better student and researcher. I also want to thank Dr. Sanjay Banerjee for his time and feedback in serving as reader of this thesis.

My fellow students have also been a tremendously valuable asset. Junghyo, En-Shao, and Babak, in particular, have helped me greatly, whether it was through discussion of my work or in teaching me the operation of essential tools. Their kindness and patience has made this experience much easier and more enjoyable. The tireless work of Kamran in setting up our NWCVD system and in the subsequent growth of high quality nanowires has been essential to my research. I would also like to thank Chris, Erica, Will, Jason, Clay, Micah, and Karun for the interesting discussions, motivation, and much-needed diversions from research.

The hard work of the technical staff and administrators has allowed me to focus on academic matters. For this I want to thank Rico, Gabriel, Melanie, Jesse, Johnny, Joyce, Gerlinde, and, especially, Jean Toll.

Without the constant support of my parents, sister, and grandparents over the years, I am sure I could not have made it as far as I have. You have my sincere gratitude

for all that you have done for me. I also want to thank my amazing girlfriend Helen for her uncanny ability to put a smile on my face, even after the longest of days spent in the lab.

August 2011

Abstract

Confined Electron Systems in Si-Ge Nanowire Heterostructures

David Carl Dillen, M.S.E.

The University of Texas at Austin, 2011

Supervisor: Emanuel Tutuc

Semiconductor nanowire field-effect transistors (NWFET) have been recognized as a possible alternative to silicon-based CMOS technology as traditional scaling limits are neared. The core-shell nanowire structure, in particular, also allows for the enhancement of carrier mobility through radial band engineering.

In this thesis, we have evaluated the possibility of electron confinement in strained Si-$Si_{1-x}Ge_x$ core-shell nanowire heterostructures. Cylindrical strain distribution was calculated analytically for structures of various dimensions and shell compositions. The strain-induced conduction band edge shift of each region was found using ***k·p*** theory coupled with a coordinate system shift to account for strain. A positive conduction band offset of up to 200 meV was found for a Si-$Si_{0.2}Ge_{0.8}$ structure.

We have also designed and characterized a modulation doping scheme for p-type, Ge-SiGe core-shell NWFETs. Finite element simulations of hole density versus radial position were done for different combinations of dopant position and concentration. Three modulation doped nanowire samples, each with a different boron doping density in the shell, were grown using a combined vapor-liquid-solid and chemical vapor deposition process. Low temperature current-voltage measurements of bottom- and top-gate samples indicate that hole mobility is limited by the proximity of charged impurities.

Table of Contents

List of Tables

List of Figures

Chapter 1: Introduction

1.1 Motivation and Background:

Throughout its lifetime, growth of the semiconductor industry has relied upon scaling of individual metal-oxide-semiconductor field effect transistors (MOSFETs) for improvements in the computational power of integrated circuits (ICs). Due to the inverse relation between MOSFET channel length and maximum cutoff frequency, this down-scaling of dimensions lead to the overall enhancement of IC performance. Fabrication costs also decrease as devices are made smaller. The shrinking of a given circuit's area requirement allows for increased production from a single wafer. The most popular method of scaling has relied on parameter (dimensions, voltage, doping) changes which maintain the device's electric field distribution between subsequent technology nodes. This allows for consistent long channel behavior even at reduced channel lengths. Under ideal constant-field scaling, also known as Dennard's scaling theory [1], all device dimensions should be reduced by a factor $1/\kappa$. Power supply voltage and channel doping must also be scaled by $1/\kappa$ and κ, respectively, in order to limit the longitudinal electric field and source to drain punch through leakage. Figure 1.1 shows the historical scaling of power supply voltage (V_{dd}), threshold voltage (V_t), and gate oxide thickness (t_{ox}) with the minimum channel length of CMOS logic devices.

Dennard's theory relies on the simultaneous, and equivalent, scaling of all device parameters. If this condition is not met, device characteristics such as threshold voltage, on-off current ratio, and even its lifetime may suffer due to deviations from ideal long

channel behavior. The balancing of threshold voltage provides an example of this necessary condition: limiting the source and drain depletion widths through the increase of channel doping requires a concurrent reduction in gate oxide thickness. Without this increased gate capacitance, the threshold voltage may rise to a point where it is incompatible with the scaled power supply voltage, limiting gate overdrive voltage and the ultimate drive current.

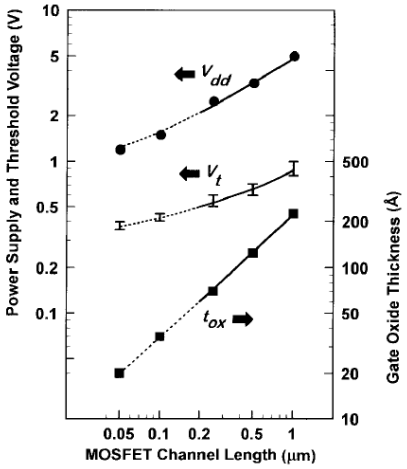

Figure 1.1. Scaling of power supply voltage, threshold voltage, and gate oxide thickness with minimum channel length for CMOS logic devices [2].

Prior to the 90 nm technology node, scaling was simply a matter of fabricating ever smaller features through advances in optical lithography combined with power supply and doping adjustments. There are now, however, a number of restrictions on further scaling, including critical voltages and dimensions which are quickly approaching fundamental limitations. After moving to sub-100 nm channel lengths, the appropriately named short channel effects became significant due to these limitations. Short channel effects generally come in two types: those related to carrier drift limitations (e.g.

saturation velocity and hot carrier effects) across the channel, and competition over channel electrostatics by the gate and drain contacts (e.g. drain induced barrier lowering and bulk punch-through).

The first category of SCE, carrier drift limitations, are the result of large longitudinal electric fields across a MOSFET's channel. As the magnitude of this field increases, carrier velocity is no longer linearly related to electric field, a situation known as velocity saturation. Large longitudinal fields, particularly near the drain junction, also produce an abundance of "hot" carriers. These energetic carriers can pass over the gate oxide's energy barrier or collide to produce electron/hole pairs through impact ionization. Continual repetition of these processes cause gate charge trapping and shifts in threshold voltage over time. Limiting the longitudinal electric field had previously been accomplished through use of the constant-field scaling theory: power supply voltage and channel length are reduced by the same factor at each technology node. This is becoming impossible as switching considerations limit the supply voltage to around one volt. Below this point, the I_{on}/I_{off} ratio suffers due to the trade-off between gate overdrive voltage (large drive current) in the on-state and the inability to drive the device well below threshold in the off-state (low standby current).

The second type of SCE results from electrostatic competition between the gate and drain terminals over the channel. In the limit of a long-channel device, the source and drain depletion widths are negligible compared to the overall channel length. As the channel length is decreased and the depletion widths become comparable to gate length,

the drain junction begins to exert control over the injection barrier at the source end. This situation, known as drain-induced barrier lowering (DIBL), leads to a large leakage current directly between the source and drain junctions, along with increased subthreshold swing. The standard prescription for this problem has relied upon thinning of the gate oxide to increase its relative capacitance over that of the drain. This has lead to extremely thin insulators of only a few atomic layers thick and the need to move to high-κ materials to prevent large gate leakage and oxide degradation.

The continual desire for increased computing power and cheaper electronics necessitates the use of new device structures if the same rapid pace of performance and packing density enhancements are expected far into the future. One such class of device is the semiconductor nanowire field-effect transistor (NWFET). This geometry, especially in the gate-all-around (coaxial) configuration, has been shown to possess improved electrostatic control over the channel, leading to the reduction of short channel effects [3] and power consumption. These factors make the NWFET an attractive prospect for post-CMOS design.

In addition to novel device designs, employing semiconducting materials other than silicon will lead to performance enhancements. Germanium has been recognized as an important material in the development of these devices, thanks in part to its excellent low-field hole mobility (~1900 $cm^2V^{-1}s^{-1}$ versus ~450 in silicon). As a group-IV material, germanium is also capable of integration with current, silicon-based CMOS technology. Silicon-germanium alloys of arbitrary composition can also be formed with key material

properties, most notably band gap and lattice constant, which gradually span the range between bulk silicon and bulk germanium.

Pseudomorphic growth of silicon/germanium heterostructures presents numerous opportunities for band- and strain-engineering of device properties. P-type devices, in particular, benefit from band engineered carrier confinement due to the large valance band offset present in this material system [4]. Core-shell nanowires have been developed which take advantage of this fact [5]. These structures feature a core of low-band gap germanium capped with a thin shell of silicon germanium. This acts to both passivate the germanium surface and confine holes to the core, spatially separating carriers from the mobility-degrading trap states at the nanowire surface. In this core-shell configuration, mobility may also benefit from the compressive strain placed on the core by the smaller lattice constant of the shell material [6].

1.2 CHAPTER ORGANIZATION:

Due to the large lattice mismatch between bulk silicon and germanium, core-shell nanowires composed of these materials and their alloys are expected to contain a significant amount of pseudomorphic strain. Chapter Two is devoted to the analytic calculation of this strain distribution throughout a core-shell heterostructure. Changes to its electronic band structure will be calculated with $k \cdot p$ perturbation theory using the calculated strain, and estimates of core to shell band offsets will be provided. The goal of Chapter Two will be to assess the possibility of core electron confinement in silicon – silicon germanium core-shell nanowires, analogous to the p-type devices discussed

above. It is expected that a tensile strained silicon core will suffer a downward shift in its conduction band minimum. Combined with the opposite effect in compressively strained silicon germanium, a type-II band alignment is predicted and has, in fact, been observed in similarly designed planar structures [7].

Chapter Three will feature the design, growth, and characterization of p-type modulation doping in core-shell nanowire heterostructures. Modulation doping, a technique which has found wide use in planar heterostructure device design, allows for the spatial separation of free carriers from ionized impurities. The overall effect is to increase drain current while minimizing mobility degradation due to charged impurity scattering. Extension of this technique to core-shell nanowire heterostructures will be accomplished by growth of an intrinsic germanium core, around which, a silicon germanium shell containing a thin, cylindrical ring of boron doping is grown. The effects of doping concentration and doped region thickness/position on free carrier concentration in the core will be determined through finite element simulation. The goal will be to optimize these parameters to allow for maximum hole transfer from shell to core, minimizing any low mobility conduction paths through the shell. Characterization of modulation doped nanowire heterostructures will be done by low temperature current-voltage measurements.

Chapter Four will serve to summarize and conclude this thesis.

Chapter 2: Strain Engineering of Core-Shell Nanowires

2.1. Introduction and Background:

Core-shell nanowires, consisting of a germanium core and a silicon germanium shell have been recognized as a desirable channel material for high mobility p-type field-effect transistors. Their benefits, discussed previously, are mainly due to the improved electrostatics of the gate-all-around structure, germanium's larger bulk mobility compared to silicon, and hole confinement which leads to a mobility enhancement by spacing carriers from the nanowire-dielectric interface. This hole confinement effect is made possible by the positive valence band offset between core and shell, approximately 250 meV for unstrained Ge-$Si_{0.5}Ge_{0.5}$.

A major drawback with this material system, however, is a lack of significant conduction band offset in any combination of unstrained silicon or germanium heterostructure. A large band offset would be desirable to create an n-type FET complementary to the p-type nanowire field-effect transistor (NWFET), while also maintaining similar values of carrier mobility. The remainder of this chapter will focus on determining the possibility of electron confinement in silicon – silicon germanium core-shell nanowire heterostructures.

The previous work by G. Abstreiter *et al.* in planar heterostructures may provide one possible solution. In 1985 they were the first to observe a two-dimensional electron gas (2DEG) in a modulation doped, Si-$Si_{0.5}Ge_{0.5}$ superlattice grown on a relaxed $Si_{0.75}Ge_{0.25}$ buffer layer [7]. Observation of this phenomenon was most likely due to improvements in growth quality over previous attempts. Their choice of buffer layer

composition meant that both layers in the superlattice would be partially strained. The type-II band alignment observed was attributed to raising the compressively strained $Si_{0.5}Ge_{0.5}$ conduction band edge combined with the opposite effect in silicon; strain magnitude was measured with Raman Spectroscopy and found to be approximately 1% in both layers. The two-dimensional nature of this electron gas was confirmed through the temperature dependence of hall mobility versus that of a control sample with Sb doping throughout the structure, not just in the SiGe spacer layers. The peak low-temperature mobility for the modulation doped structure was about an order of magnitude larger than in the control, indicating spatial separation of carriers from ionized dopants and confinement to the silicon layers. Observations of Shubnikov-de Haas oscillations in the sample's magnetoresistance also provide evidence for two dimensional transport since these were only visible when the magnetic field was aligned perpendicular to the plane of the superlattice.

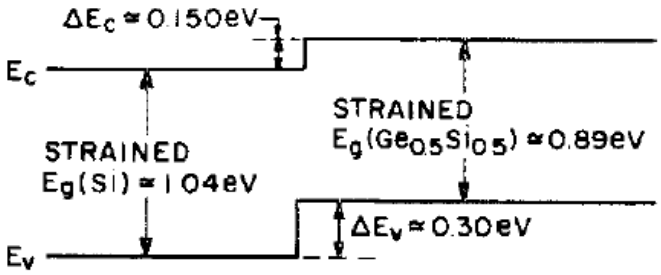

Figure 2.1. Band alignments of a $Si/Si_{0.5}Ge_{0.5}$ heterostructure grown on a relaxed $Si_{0.75}Ge_{0.25}$ buffer layer [4].

R. People and J. C. Bean used phenomenological deformation potential theory calculations and estimated the conduction band offset to be 150 meV in a biaxially

strained $Si/Si_{0.5}Ge_{0.5}$ heterostructure grown on a fully relaxed $Si_{0.75}Ge_{0.25}$ buffer layer [4], shown in Figure 2.1. Since this discovery, many groups have demonstrated high mobility and high transconductance in n-type modulation-doped field-effect transistors (MODFETs) to exhibit the benefit of this structure for device applications. The device of [8] features a 1.4 μm recessed gate to increase the intrinsic transconductance to 800 mS mm^{-1} at 77˚K. Also noted was the large electron Hall mobility of 15,700 $cm^2V^{-1}s^{-1}$ at 77˚K.

Electron confinement is not the only benefit that is possible in such a structure. The electron mobility in silicon has been shown to increase with certain types of strain, due mainly to the reduced intervalley scattering rate between once equivalent valleys. Strain can be either biaxially applied at the wafer level, such as the Si-SiGe heterostructures seen previously, or through uniaxial post-fabrication techniques. The post-fabrication straining of MOSFET devices had even been commercialized in Intel microprocessors since 2005 in their 90 nm node. This was accomplished through application of a silicon nitride capping layer which provided uniaxial tensile strain across the channel. Strained Si/Ge heterostructures have been shown to provide greater than 100% mobility enhancement over unstrained, bulk materials for both types of carriers [6].

The case of a Si-SiGe core-shell nanowire is expected to be similar to the planar structures discussed above. A nanowire core possesses an elastic compliance much larger than that of a true substrate, meaning both the core and the shell will share a portion of the lattice mismatch. If this is correct, the possibility of radial electron confinement is real

and will allow for strain engineering of energy bands, including the maximization of band offset and the correspondingly enhanced electron mobility in tensile-strained Si. Consequently, calculating the strain distribution in such a nanowire provides valuable insight into the optimization of growth parameters such as core radius, shell thickness, and material concentration. These calculations will be the topic of the Section 2.3. Section 2.2 provides an overview on stress and strain. The band structure changes due to the calculated strain distribution will be discussed in Section 2.4. Section 2.5 discusses future work in this subject.

2.2. BASIC STRESS/STRAIN RELATIONSHIPS AND DEFINITIONS:

Elastic strain is defined as the deformation of a body due to a force applied at its surface. It is usually expressed as a second rank tensor, either unitless or as a percentage value:

$$\varepsilon_{ij} = \begin{bmatrix} \varepsilon_{xx} & \varepsilon_{xy} & \varepsilon_{xz} \\ \varepsilon_{yx} & \varepsilon_{yy} & \varepsilon_{yz} \\ \varepsilon_{zx} & \varepsilon_{zy} & \varepsilon_{zz} \end{bmatrix} \tag{2.1}$$

The indices above correspond to the direction of force and the surface normal on which it is acting, e.g. ε_{yx} indicates a deformation in the y direction of a surface whose normal faces x. Terms along the main diagonal of Eq. (2.1) are known as the normal components of strain since they result in only volume changes in the material. Off-diagonal terms are shear strains, producing changes in bond angle only. The requirement that there be no rigid body translations or rotations forces off-diagonal shear terms to be symmetric, e. g. $\varepsilon_{yx} = \varepsilon_{xy}$. The sign of strain indicates the type of deformation present: a negative value

designates compressive strain, while positive strain is tensile in nature.

Stress is directly related to strain through Hooke's Law:

$$\sigma_{ij} = \sum_{k,l=1}^{3} C_{ijkl}\varepsilon_{kl} \tag{2.2}$$

where C_{ijkl} are the material's elastic stiffness constants, forming a fourth rank tensor of 81 terms. The specific crystal symmetry reduces the required number of terms to two for an isotropic material and three for cubic structures. Stress, a second rank tensor, is expressed in units of Pascals and can be thought of as pressure in a material due to an applied force. As in the strain tensor, stress must also be symmetric to avoid rigid body movement.

Another term of interest is displacement, a vector field defining the change in position of a given point between the strained and unstrained cases. Displacement, $\boldsymbol{u}$, and strain are linked through the relation:

$$\varepsilon_{ij} = \frac{1}{2}\left(\frac{du_i}{dx_j} + \frac{du_j}{dx_i}\right) \tag{2.3}$$

The stress/strain tensors above were given in Cartesian coordinates; however, practical calculations often rely on cylindrical coordinates to take advantage of the natural symmetry of the nanowire structure.

A few technologically important cases are that of biaxial, uniaxial, and hydrostatic strain. Biaxial strain, such as in a planar heterostructure, stretches or contracts the material in the plane of growth while allowing it to respond freely in the remaining direction. Similarly, uniaxial strain is along one direction only. The material may then relax freely in the opposing directions. Hydrostatic strain is defined as the sum of the

three normal strain components: $\varepsilon_H = \mathrm{Tr}(\varepsilon_{ij}) = \varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}$. It is directly related to the volume change of a strained body. Since only atomic bond lengths are altered, crystal symmetry and corresponding band degeneracies remain intact.

2.3. Strain Calculation Methods for Core-Shell Nanowires:

A number of strain calculation methods for core-shell nanowires have been published recently. These come in three classes: finite-element modeling, atomistic models, and analytical solutions.

2.3.1 Strain Modeling by Finite-Element Analysis:

Finite-element modeling of strain, such as in the work by Søndergaard, *et al*. [9], uses discrete meshing of a nanowire, over which the total elastic energy of the structure is minimized. Elastic energy, U, is expressed as:

$$U = \int w\, dV = \frac{1}{2}\int \sum_{ijkl} C_{ijkl}\varepsilon_{ij}\varepsilon_{kl}\; dV \tag{2.4}$$

where w is the strain energy density and other variables take their usual meaning. Initial conditions are given such that the core is unstrained and the lattice mismatch is fully taken up by the shell, clearly not the lowest energy configuration. The displacement field is then varied to relax the shell's initial strain and minimize Eq. (2.4).

If an infinitely long nanowire is assumed, the problem reduces to a two-dimensional cross section with only one parameter describing the axial strain of the entire structure. This assumption was shown by the authors in [9] to be very close to the results obtained for a three-dimensional structure if the ends of the nanowire are not considered.

Other than this, no other simplifying assumptions must be made and any arbitrary crystal structure can be used as long as its elastic constants are known.

Figure 2.2 shows sample finite-element calculation results for a hexagonal nanowire with a GaAs (a = 0.565 nm) core and GaP (a = 0.545 nm) shell. The z-axis is defined as the direction of growth, [111]. The normal components of strain, ε_{xx} and ε_{yy}, have complicated distributions individually, but when summed with ε_{zz} to give hydrostatic strain lead to a nearly constant value in either region. For this case ε_H = -4.4% in the entire core and 0.8% throughout much of the shell. Calculations for cylindrical cross-sectioned nanowires were said to have qualitatively similar results, but were not explicitly shown [9]. The large difference in strain magnitude between the core and the shell is due to the comparatively thick shell used: 13.9 nm radius versus 6.0 nm for the core; use of a thinner shell is expected to distribute strain more evenly throughout the structure.

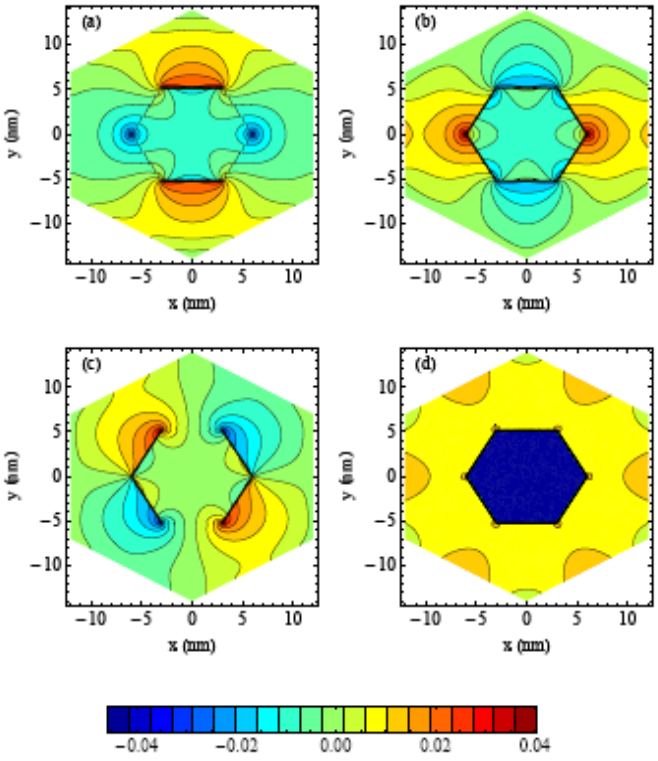

Figure 2.2. Strain component distribution in a GaAs core – GaP shell nanowire: (a) ε_{xx}, (b) ε_{yy}, (c) ε_{xy}, and (d) Tr{ε}. Core and shell radius were 6.0 nm and 13.9 nm. [9]

2.3.2 Atomistic Strain Calculations:

Grönqvist, et al, present atomistic calculations, based on Valence-Force Field models, and a comparison of the results to those of finite-element analysis [10]. This model builds up a given crystal structure atom by atom and uses the individual atomic positions in a given unit cell as the degrees of freedom to minimize elastic potential energy. This model is extremely robust, even allowing for heterostructures between materials of different crystal structures.

The difficulty in implementing this model comes from reconciling the continuum,

macroscopic nature of strain with the atomic solutions obtained. Extra steps must be added to convert local atomic bond lengths and angles into a useful strain tensor. Results often display a roughness on the atomic scale where neighboring atoms may have much different strain values, requiring some form of numerical averaging. The elastic constants of a material are also a strictly macroscopic concept. Atomistic coupling constants in [10] were extracted from comparison to finite-element models which were also used. This greatly complicates the extension of this model to other material combinations.

Comparison between finite-element and atomistic solutions showed remarkably similar results, indicating that the increased numerical robustness of the VFF model is unnecessary. This is especially true when considering the extra computational time required.

2.3.3. Analytical Calculations of Strain Distribution:

The final model we discuss is one which calculates the strain distribution of a core-shell nanowire analytically. The following is based closely on the work of V. Schmidt, et al. [11]. Summing the forces on an infinitesimal body in a single direction gives the equation of motion for that body:

$$\frac{d\sigma_{11}}{dx_1} + \frac{d\sigma_{12}}{dx_2} + \frac{d\sigma_{13}}{dx_3} + \rho g_1 = \rho a_1 \tag{2.5}$$

where ρ is the material density, g is gravity or other external forces, and a_1 is acceleration in the direction of index one. These calculations will assume a free standing body with no external forces acting on it, causing g and a to take a value of zero. These changes, along with generalization to three dimensional space, produces:

$$\nabla \cdot \sigma_{ij} = 0 \tag{2.6}$$

Eq. (2.6) is known as the equation of equilibrium and is the starting point for this calculation.

A number of assumptions must be made to make this problem more tractable. The first is the assumption that the material's elastic properties are isotropic and can be described by only two constants, Poisson's ratio υ and the shear modulus G. Furthermore, these constants will be assumed to be equal in core and shell regions, although the model may be generalized to account for any significant differences. An infinitely long nanowire is also assumed. The requirement of translational invariance means the radial displacement, u_r, does not change with axial position and the axial displacement, u_z, does not change with radial position. The cylindrical symmetry of the core-shell structure allows for neglecting of the angular component of displacement, u_φ, along with any positional derivative with respect to φ.

When the above assumptions are implemented, the equation of equilibrium is condensed down to two independent equations, one for the radial direction and one for the axial direction:

$$\frac{d^2 u_r^{(a)}}{dr^2} + \frac{1}{r}\frac{du_r^{(a)}}{dr} - \frac{u_r^{(a)}}{r^2} = 0 \tag{2.7a}$$

$$\frac{d^2 u_z^{(a)}}{dz^2} = 0 \tag{2.7b}$$

The superscript index α has been introduced to denote the region to which the variable applies, one for the core and two for the shell. The general solutions to these equations

have the form:

$$u_r^{(a)} = a^{(a)} r + \frac{b^{(a)}}{r} \tag{2.8a}$$

$$u_z^{(a)} = c^{(a)} z \tag{2.8b}$$

leaving six constants to be solved for based on boundary condition arguments.

The first boundary conditions to consider are displacements at the core/shell interface. Axial displacement in the core must equal that in the shell assuming pseudomorphic shell growth. The same is true of radial displacements at the interface.

The net force in the radial direction at the core/shell interface must vanish, leading to the relation that $\sigma_{rr}^{(1)}(R_1) = \sigma_{rr}^{(2)}(R_1)$, where R_1 is the core radius. The net force in the axial direction must also equal zero: integrating the force over a given cross section yields $R_1^2\sigma_{zz}^{(1)} + (R_2^2\text{-}R_1^2)\sigma_{zz}^{(2)} = -2\tau R_2$. Surface stress, τ, has been introduced; it is defined as the work done in changing surface area through elastic strain. R_2 is total radius of the core-shell structure. The finally boundary condition is zero force in the radial direction at the shell's outer surface, requiring that $\sigma_{rr}^{(2)}(R_2) = -\tau/R_2$. Use of the above relations lead to the following solutions for the six unknowns:

$$a^{(1)} = \frac{m(1-3v)(R_2^2 - R_1^2)}{2(1-v)R_2^2} - \frac{\tau(1-3v)}{2G(1+v)R_2} \tag{2.9a}$$

$$a^{(2)} = \frac{m[2R_2^2(1-v) - R_1^2(1-3v)]}{2(1-v)R_2^2} - \frac{\tau(1-3v)}{2G(1+v)R_2} \tag{2.9b}$$

$$b^{(1)} = 0 \tag{2.9c}$$

$$b^{(2)} = \frac{-m(1+v)R_1^2}{2(1-v)} \tag{2.9d}$$

$$c^{(1)} = c^{(2)} = \frac{m(R_2^2 - R_1^2)}{R_2^2} - \frac{\tau(1-v)}{G(1+v)R_2} \qquad (2.9e)$$

Variable *m* above is the lattice mismatch factor and is defined as the difference in lattice constant between the shell and core, divided by the core's constant. From the displacement-strain relation of Eq. (2.3), strain components can now be calculated from the six constants of Eq. (2.9 a-e):

$$\varepsilon_{rr}^{(1)} = a^{(1)} \qquad (2.10a)$$

$$\varepsilon_{rr}^{(2)} = a^{(2)} - m - \frac{b^{(2)}}{r^2} \qquad (2.10b)$$

$$\varepsilon_{zz}^{(1)} = c^{(1)} \qquad (2.10c)$$

$$\varepsilon_{zz}^{(2)} = c^{(2)} - m \qquad (2.10d)$$

With all other strain components equal to zero.

2.3.4 Strain Calculation Results for Si-SiGe Core-Shell Nanowire Heterostructures:

The analytical model of Section 2.3.3 was chosen for determining the strain distribution in a silicon core, silicon-germanium shell nanowire heterostructure mainly because of its ease of implementation. The use of isotropic material parameters in describing a region's elastic properties was deemed reasonable since the nanowires of interest are cylindrical in nature and only the growth direction, [111], is known. Any external or interface surfaces, instead, feature a combination of many undefined planes. The average result will therefore appear isotropic, allowing the use of elastic moduli constants, υ and *G*. The differences in these values between silicon and germanium are largely insignificant, validating the use of only one set of elastic constants throughout the

entire structure. The other assumptions were considered less important, such as the use of an infinitely long nanowire. This is expected to give accurate values away from the ends of a finite nanowire.

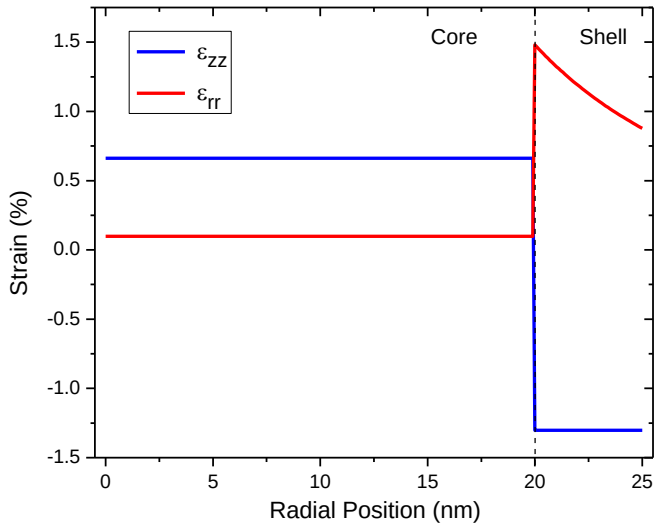

Figure 2.3. Radial (red) and axial (blue) strain distribution versus radial position in a Si-Si0.5Ge0.5 core-shell nanowire with 20 nm core radius and 5.0 nm shell thickness.

Strain components were calculated using Eq. (2.10 a-d) for Si-$Si_{0.5}Ge_{0.5}$ core-shell nanowires with total outer radius between 15 and 35 nm, shell thicknesses of 2.5, 5.0, and 7.5 nm were used. Elastic constants were taken to be G = 52 GPa and υ = 0.26 [12]. A surface stress value of 1 N/m was used [11], an average of values cited in the literature.

Strain distribution inside a structure with core radius 20 nm and a shell thickness of 5.0 nm is shown versus radial position in Figure 2.3. As expected from the infinite length assumed, axial strain is constant in both the core, 0.66%, and the shell, -1.30%, with a discontinuity at the interface. Radial strain is also constant in the core, 0.10%

throughout. Only the radial strain component in the shell is shown to depend on position. In this case it starts at 1.48% at the interface and reduces to 0.88% at the outer wall.

It should be noted that all strain components in the core are tensile, a case not seen in planar epitaxial growth schemes. There, the material always has one free direction to minimize its elastic energy: a biaxially strained layer can freely expand or contract out of the plane of growth. This, however, is not the case for a core shell nanowire. As the silicon core is stretched axially by the larger lattice constant silicon germanium shell, it would normally contract in the radial direction. Since the core is also constrained radially, it cannot do this.

Individual strain components for different core/shell size combinations are summarized in Figure 2.4 a-c). Note that only strain's magnitude is shown; axial strain in the shell is compressive while all others are tensile. The value chosen here for radial shell strain was its maximum at the core/shell interface.

It was found that radial strain does not change significantly with nanowire dimensions. In the shell, radial strain only ranges from 1.42 to 1.59% over all size combinations, while nearly vanishing in the core, 0.03 to 0.21%.

Axial strain has a much larger dependence on nanowire dimensions. For a given shell thickness, axial strain in the core will decrease with an increasing nanowire radius. The opposite is true in the shell. Similarly, by increasing shell thickness, the core's axial strain will increase, while the shell's is shown to decrease. These relationships are consistent with the expectation of decreasing elastic compliance in a material as its size is

increased, causing the opposite material to bear a greater amount of total stress.

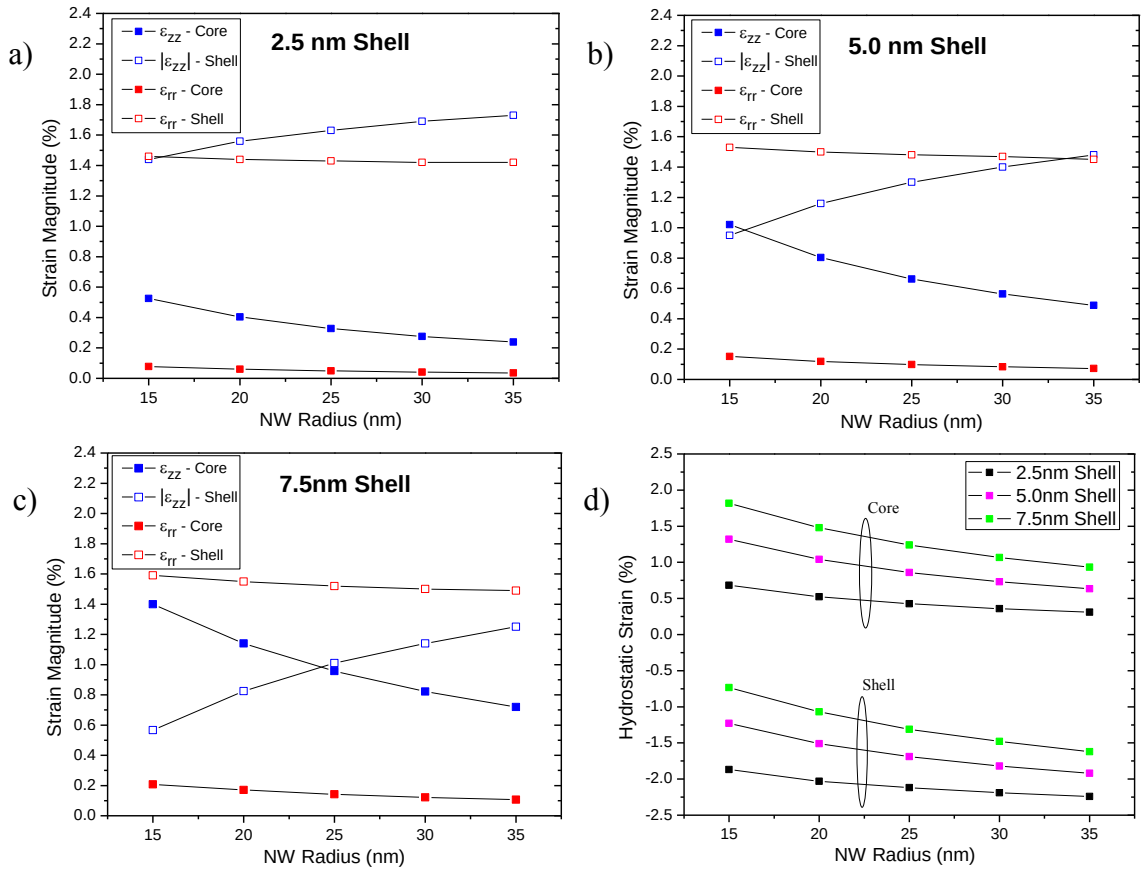

Figure 2.4. Components of strain magnitude in a Si-$Si_{0.5}Ge_{0.5}$ core-shell nanowire with variable outer radius and a) 2.5 nm, b) 5.0 nm, and c) 7.5 nm shell thickness. Axial strain in the shell is compressive, all others are tensile. The maximum value of radial shell strain was used in a-c. Total hydrostatic strain is shown in d) for each core/shell size combination tested.

Hydrostatic strain, introduced in Section 2.2, is the sum of the three Cartesian normal strain components and is related to the total volume change of a given body. Since cylindrical strain components have been calculated, they must now be converted to Cartesian components in a nanowire oriented coordinate system in order to use previously developed models to describe strained band structure changes. This new

coordinate system is aligned with the z-direction along the nanowire axis and x, y arbitrarily placed orthogonally to the main axis. The conversion is straightforward, beginning with the x and y displacement fields:

$$u_x^{(a)} = u_r^{(a)} \cos(\varphi) = a^{(a)} x + b^{(a)} \frac{x}{x^2 + y^2} \tag{2.11a}$$

$$u_y^{(a)} = u_r^{(a)} \sin(\varphi) = a^{(a)} y + b^{(a)} \frac{y}{x^2 + y^2} \tag{2.11b}$$

Strain can then be calculated through the strain-displacement relation of Eq. (2.3). Due to different geometries in the core and shell, strain components in each region have dissimilar forms:

$$\varepsilon_{xx}^{(1)} = \varepsilon_{yy}^{(1)} = a^{(1)} \tag{2.12a}$$

$$\varepsilon_{xx}^{(2)} = a^{(2)} + b^{(2)} \frac{(y^2 - x^2)}{(x^2 + y^2)^2} - m \tag{2.12b}$$

$$\varepsilon_{yy}^{(2)} = a^{(2)} + b^{(2)} \frac{(x^2 - y^2)}{(x^2 + y^2)^2} - m \tag{2.12c}$$

Axial strain is equivalent in both coordinate systems and is left in its original form. When put in terms of the original cylindrical components, hydrostatic strain takes the form:

$$\varepsilon_H^{(1)} = 2\varepsilon_{rr}^{(1)} + \varepsilon_{zz}^{(1)} \tag{2.13a}$$

$$\varepsilon_H^{(2)} = 2\left(\varepsilon_{rr}^{(2)} + \frac{b^{(2)}}{r^2}\right) + \varepsilon_{ZZ}^{(2)} = 2\left(a^{(2)} - m\right) + \varepsilon_{ZZ}^{(2)} \tag{2.13b}$$

where its distribution becomes constant in both the core and the shell for any given size combination.

Values of hydrostatic strain are shown in Figure 2.4 d) for a Si-$Si_{0.5}Ge_{0.5}$ core-shell nanowire of varying dimension. An interesting result is that the difference between the core and the shell's hydrostatic strain is a constant 2.55%, independent of nanowire size. This may be beneficial in that the ultimate conduction band offset will not be significantly affected by small size variations between nanowires, or by the natural tapering of vapor-liquid-solid (VLS) grown nanowires.

Hydrostatic strain was calculated next for nanowires of varying shell composition. The case of a Si-$Si_{1-x}Ge_x$ core-shell nanowire with 20 nm core radius and 5.0 nm shell thickness is shown in Figure 2.5. For each composition tested, the difference in hydrostatic strain between core and shell is always independent of nanowire size, as seen previously. Now, however, this difference relies on the shell's composition, ranging from 0.0% at x = 0.0 to 5.42% at x = 1.0.

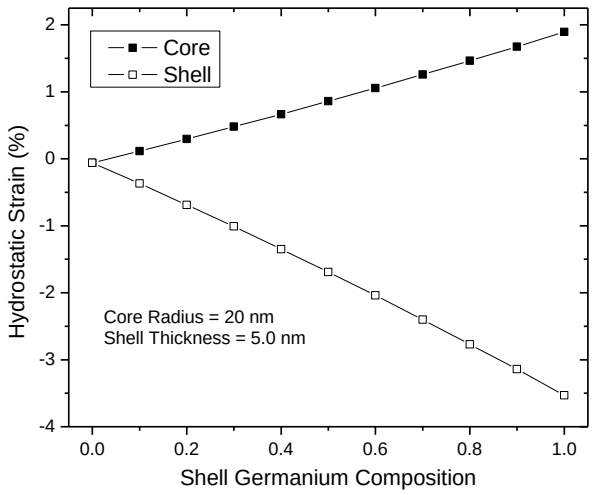

Figure 2.5. Hydrostatic strain in a Si-$Si_{1-x}Ge_x$ core-shell nanowire of varying shell composition. The core radius is 20 nm and the shell's thickness is 5.0 nm.

2.4 Calculation of the Strain-Induced Conduction Band Shift:

Through changes in interatomic bond lengths and angles, strain can have a tremendous effect on a material's band structure. Seen previously in the [7], biaxially strained Si-$Si_{0.5}Ge_{0.5}$ superlattices were shown to shift to a type-II band alignment, allowing for electron confinement into the silicon layers. A number of different band structure calculation methods have been developed for treatment of strained crystals, most notable are the tight-binding and ***k•p*** framework.

The tight-binding method uses orbital overlap parameters to express valance electron coupling between nearest neighbors. Solutions are relatively simple when only a few atomic orbitals are included, giving acceptable results for the valance bands. However, when properly account for the higher lying bands, less localized orbitals must be considered and the problem size increases significantly. Including strain also requires that an entirely different crystal structure be developed. For a more accurate treatment of strained band structures, the ***k•p*** method will be introduced here.

2.4.1 Introduction to the *k•p* Method for Band Structure Calculations:

The ***k•p*** method is a perturbation-based theory. Empirical parameters are used to determine band energies at high symmetry points in k-space. Moving away from these points by a small amount is the perturbation added to the original Hamiltonian. The band structure around points of high symmetry in k-space can be expressed using a relatively small basis set, allowing for a quick and accurate outcome. Strain is also easy to incorporate, unlike with the tight-binding method. It is treated as an additional perturbation to the unstrained Hamiltonian, with a shift in coordinate system due to

deformation in the crystal.

The unstrained ***k•p*** Hamiltonian can be expressed as [13]:

$$\left[\frac{p^2}{2m_0} + V(\boldsymbol{r}) + \frac{\hbar^2 k^2}{2m_0} + \frac{\hbar}{m_0}\boldsymbol{k}\cdot\boldsymbol{p}\right] u_{n\boldsymbol{k}}(\boldsymbol{r}) = E_n(\boldsymbol{k}) u_{n\boldsymbol{k}}(\boldsymbol{r}) \tag{2.14}$$

where $u_{nk}(r)$ are the Bloch states of the nth band with wave vector k. The solution is first established for a single point, $k = k_0$. Adjacent k-points can subsequently be solved for by a linear expansion of this solution around $k = k_0$.

For the addition of strain to Eq. (2.14), the method of Pikus-Bir is often used [14]. A deformed crystal structure will have a modified periodic potential and boundary conditions from that of the original crystal. This fact requires the use of a transformation between coordinates of both cases:

$$r'_i = r_i + \sum_j \varepsilon_{ij} r_j \tag{2.15}$$

where r'_i is the deformed coordinate and ε_{ij} is the strain tensor. Utilizing this transformation, the strained Pikus-Bir Hamiltonian becomes:

$$\left[\frac{p^2}{2m_0} + V(\boldsymbol{r}) + \frac{\hbar}{m_0}\boldsymbol{k}\cdot\boldsymbol{p} + \frac{\hbar^2 k^2}{2m_0} + H_\varepsilon + H_{\varepsilon\boldsymbol{k}}\right] u'_{n\boldsymbol{k}}(\boldsymbol{r}) = E_n(\boldsymbol{k}) u'_{n\boldsymbol{k}} \tag{2.16a}$$

$$H_\varepsilon = \sum_{i,j}\left(-\frac{1}{m_0} p_i p_j + V_{ij}\right)\varepsilon_{ij} \tag{2.16b}$$

$$H_{\varepsilon k} = -\frac{2\hbar}{m_0}\sum_{i,j} k_i \varepsilon_{ij} p_j \tag{2.16c}$$

The V_{ij} term above is the derivative of the original periodic potential with respect to the strain tensor; all other variables have their usual meanings. Use of this method requires

that the strain tensor is homogeneous across a structure, or at least slowly varying, in order to maintain the applicability of Bloch's Theorem in the final results. The solution of this problem is similar to the previous case, except now the unstrained results are expanded in terms of a perturbative strain. Whereas the expansion in k earlier was done to second order, only a first order correction due to strain is necessary.

When this problem is solved for the shift in energy of a conduction band edge due to strain, the following form is obtained [15]:

$$\Delta E_c^i = \left(\Xi_d^i \bar{\bar{1}} + \Xi_u^i \{\hat{\boldsymbol{a}}_i \hat{\boldsymbol{a}}_i\}\right) : \bar{\bar{\varepsilon}} \tag{2.17}$$

where $\boldsymbol{a}_i$ is a unit vector parallel to the direction of energy valley i, Ξ^i_{d} and Ξ^i_{u} are the dilation and uniaxial deformation potentials of the conduction band, respectively. Indirect gap semiconductors, such as silicon and germanium, require the use of two conduction band deformation potentials to account for energy splitting of equivalent valleys due to uniaxial and shear strain components. Direct gap materials need only one parameter, a_c, as only hydrostatic strain can significantly change their band structure. Solving for the average shift in conduction band energy of an indirect gap material due to hydrostatic strain results in the following equation:

$$\Delta E_{c,av} = \left(\Xi_d^i + \frac{1}{3}\Xi_u^i\right)\varepsilon_H \tag{2.18}$$

The term in parentheses is often referred to as the average conduction band deformation potential for an indirect gap material. The conduction band deformation potential values for silicon and germanium are shown in Table 2.1. The superscript notation indicates which conduction band valley the value corresponds to.

Material	Ξ^{Δ}_{d} (eV)	Ξ^{Δ}_{u} (eV)	Ξ^{L}_{d} (eV)	Ξ^{L}_{u} (eV)
Si	-0.43	8.94	-6.59	15.5
Ge	-3.02	8.81	-9.09	15.7

Table 2.1. Conduction band deformation potentials for the Δ and L valleys of Si and Ge. [13] [15] [16] [17] [18]

2.4.2 Conduction Band Energy Shift in Core-Shell Nanowires:

The deformation potentials of Eq. (2.17) and Table 2.1 are defined in a crystal-oriented coordinate system (x = [100], y = [010], and z = [001]). Therefore, the Cartesian strain tensor calculated in Section 2.3.4, ε_{kl}, must now be converted to this new coordinate system, ε'_{ij}, through the relation of Eq. (2.19a) and the tensor transformation matrix of Eq. (2.19b). The nanowire is aligned with its main axis along the crystal [111] direction and the previous *x,y* axes are assumed as the new [1-10] and [11-2] directions, respectively.

$$\varepsilon'_{ij} = \sum_{k,l} a_{ik} a_{jl} \varepsilon_{kl} \tag{2.19a}$$

$$a_{ik} = \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{3}} \\ \frac{-1}{\sqrt{2}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{3}} \\ 0 & \frac{-2}{\sqrt{6}} & \frac{1}{\sqrt{3}} \end{bmatrix} \tag{2.19b}$$

Since the band shift due to strain is calculated with respect to the original, unstrained energy, knowledge of the relative band alignments of silicon and germanium in the absence of strain is necessary. However, this parameter is not well defined in literature as there is difficulty in determining a constant energy reference level across a

hetero-interface. Morar, et al. [19] use core-level electron-energy-loss spectroscopy (EELS) of bulk $Si_{1-x}Ge_x$ alloys to provide insight into unstrained band alignments. It was proposed that the silicon $2p_{3/2}$ core-level will remain constant across a $Si_{1-x}Ge_x$/ $Si_{1-y}Ge_y$ interface of arbitrary compositions x and y. Measurement of the $2p_{3/2}$ to conduction band transition energy results in the values for $\delta E_{c,0}$ used in these calculations, shown as black squares in Figure 2.6 b). These unstrained offsets were used as the basis for test calculations of conduction band offset in a biaxially strained $Si_{1-x}Ge_x/Si_{1-y}Ge_y$ heterostructure of varying composition, x and y. Results were in good agreement with the nonlocal empirical pseudopotential calculations of [16].

Shell-to-core conduction band offset may now be calculated based on the crystal-oriented strain tensor from above, the ***k•p*** band structure theory of Section 2.4.1, and the unstrained band alignments from [19]. Deformation potential values for silicon and germanium were given in Table 2.1, a linear distribution between these values is assumed for the alloyed shell. Two sets of constants are needed in each material to describe the shift in both the Δ and L valleys of each. The strain distribution is assumed to be constant or slowly varying across the structure to allow for use of the periodic, strained crystal potential in Eq. (2.16). To provide an accurate picture of band offset in these structures, both average conduction band energy and band splitting due to shear strain will be calculated. Any energy splitting that is present will act to decrease the actual conduction band offset between core and shell. The energies of the six conduction band **Δ**-valley and eight L-valleys were calculated point-by-point in the core-shell structure with MATLAB.

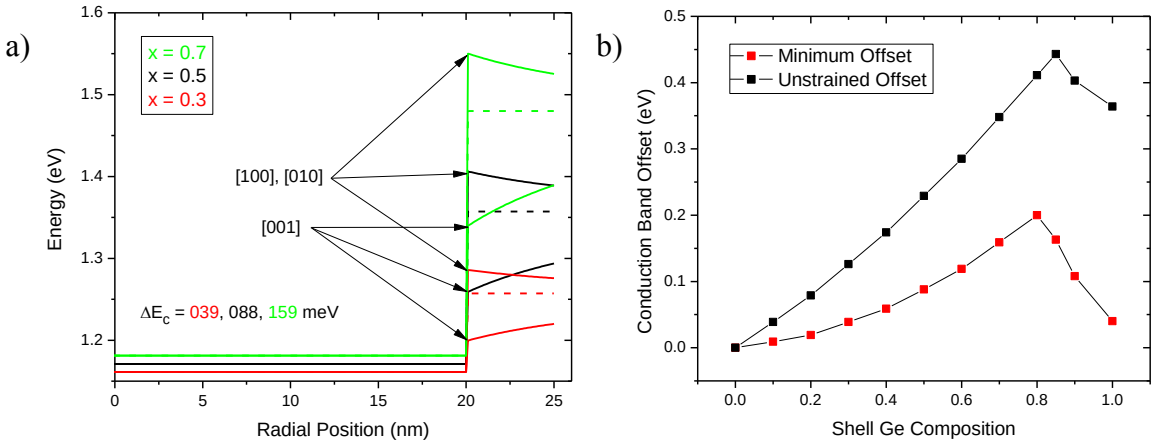

Figure 2.6. a) Conduction band *Δ*-valley edges versus radial position for a Si- $Si_{1-x}Ge_x$ core-shell nanowire with 20 nm core radius and 5.0 nm shell thickness. Data for x = 0.3, 0.5, and 0.7 is shown and dashed lines indicate average C.B. energy. Split bands are labeled with their valley direction. b) Minimum (red) and unstrained (black) conduction band offsets as a function of shell composition. Unstrained offset data from [19].

Figure 2.6 a) shows three sets of conduction band (*Δ*-valley) edges versus radial position for a Si-$Si_{1-x}Ge_x$ nanowire with 20 nm core radius and a 5.0 nm shell thickness. Green lines show a shell of composition x = 0.7, while black and red correspond to x = 0.5 and 0.3, respectively. Dashed lines indicate the average *Δ*-valley energy in the shell. As expected, conduction band energy in the core remains degenerate. Symmetry in silicon's conduction band minima, along <100> directions, ensure that the core's [111] axial strain would not cause splitting of its six equivalent valleys. Combined with nearly vanishing radial strain, this results in negligible valley splitting in the core. The situation of the shell differs due to the large magnitude of radial (shear) strain present. Conduction bands are seen to split into degenerate [100] and [010] valleys and a [001] valley at lower energy, separated by over 200 meV at the core-shell interface for a shell of large

germanium composition. Since band shift calculations take into account the crystal orientation of the nanowire, conduction band energy is no longer angularly uniform around the shell. Data of Figure 2.6 corresponds to the radial slice showing the lowest conduction band energy in the shell, providing the "worst case" core to shell band offset.

Conduction band offset was found for a $Si_{1-x}Ge_x$ shell composition covering the entire range from silicon to germanium for a core-shell nanowire with 20 nm silicon core radius and a 5.0 nm shell thickness. Results are shown in Figure 2.6 b) for the minimum (red circles) band offset as a function of shell composition. Unstrained conduction band offset (black squares) has also been included as reference. Minimum band offset was seen to monotonically increase from 0.0 eV in the case of a pure silicon shell to 200 meV at x = 0.8. At this point, the $Si_{1-x}Ge_x$ shell becomes germanium-like in its conduction band character, with energy valleys along the <111> directions [20]. Unstrained band offset actually begins to decrease as x is increased, causing an abrupt decline in minimum offset when increased band splitting is considered. For comparison to planar results, a Si-$Si_{0.5}Ge_{0.5}$ nanowire shows a minimum offset of 88 meV, while the same biaxially strained structure of [4] increases to 150 meV. It is clear that the large radial strain in the shell leads to severe conduction band splitting in that region. The offset is decreased from unstrained values due to the sharp increase in band splitting with strain, which acts to negate any rise in average conduction band position.

Core/shell dimensions were largely inconsequential in the calculated minimum offset, changing it by less than 3 meV across the entire size range of Figure 2.4. Shell

composition is by far the main factor in the conduction band offset, leading to only slight variation in offset due to size fluctuations and the natural tapering of VLS-grown nanowires.

2.5 FUTURE WORK:

2.5.1 Growth and Characterization of Si-SiGe Core-Shell Nanowires:

The next stage in this project is to grow a sample of Si-$Si_{1-x}Ge_x$ core-shell nanowires for subsequent electrical characterization. Mobility measurements in such a sample could help to determine if electron conduction is predominately through the core, indicating confinement and the expected type-II band structure.

Nanowire growth will be accomplished through the Vapor-Liquid-Solid (VLS) mechanism [21] in an ultra high vacuum chemical vapor deposition (UHV-CVD) system. VLS growth relies on a metal catalyst, typically gold, deposited on the substrate wafer's surface. When heated in a hydrogen ambient to roughly 500˚C this thin metal layer will coalesce into liquid droplets, their size controlled by the time and temperature of anneal used. A gaseous silicon precursor, silane, is then introduced into the UHV-CVD chamber. Growth temperature is chosen to be below that needed for planar CVD deposition of silicon across the wafer surface. At this temperature, precursor decomposition and silicon incorporation into the gold droplets must be possible; 500˚C has been shown to work well for silane. During initial stages of growth the silicon concentration in the droplet will continue to rise until it becomes supersaturated, shown in Figure 2.7 a). At this point, solid silicon will precipitate out of the Au-Si alloy at the solid-liquid interface, causing

vertical growth of the nanowire in the same surface orientation as the substrate wafer, Figure 2.7 b). Proper control of temperature and pressure throughout the growth process will ensure predominately vertical nanowires with minimal sidewall deposition.

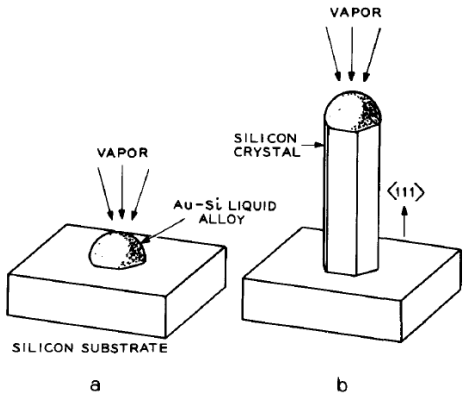

Figure 2.7. Representation of vapor-liquid-solid growth of a silicon nanowire. a) Initial precursor decomposition and alloy formation and b) vertical nanowire growth showing catalyst travelling vertically with the nanowire tip [21].

With the silicon core at its final length, shell growth can begin. Temperature is increased to favor conformal CVD growth, as opposed to the VLS method used in the core. Silane and germane are simultaneously introduced into the chamber for growth of SiGe, their relative flow rates will determine the final composition of the shell. When the shell reaches its desired thickness, gas flow is stopped and the wafer is cooled.

A modulation doping scheme may also be used in these nanowires. Essentially, a thin layer of donor dopants is included at the center of the shell, where conduction is not expected. The benefit of this is to increase the total carrier concentration in the core while minimizing charged impurity scattering due to spatial separation. Modulation doping was used by the authors in [7] to help confirm the type-II band offset in the strained Si-SiGe

planar heterostructure: these samples showed large mobility enhancement over devices with doping throughout, indicating electron confinement. Modulation doping in core-shell nanowires will be the topic of the next chapter.

Similar measurements of electron mobility in Si-SiGe core-shell nanowires may also help to confirm or disprove the presence of electron confinement in such a structure. When compared side-by-side to bare silicon nanowires of similar size, increased mobility is expected in the core-shell based nanowires. This may be due to many different factors working together, including the separation of free carriers from surface trap states and any mobility enhancements directly as a result of strain (not confinement based). Low temperature measurements can help to shed light on the relative importance of various scattering mechanisms, whether it is from phonons, charged impurities, or alloy scattering in silicon germanium.

2.5.2 Nanowire Strain Measurements Using Raman Spectroscopy:

The strain distribution in a Si-SiGe core-shell nanowire was calculated analytically in Section 2.3.4. Direct measurement of the strain present could provide experimental verification of these calculation results, Raman spectroscopy is one possible solution for this.

In this technique, inelastic scattering of visible light is used to probe the vibrational state of a material. Excitation radiation below the absorption threshold of the sample is usually used in order to minimize electronic transitions. When excited with such a source, electrons are promoted to short lived virtual states where energy is quickly

dissipated through photon emission. In most cases, the incident and emitted photons are of the same energy, known as elastic Rayleigh scattering. However, the electron may also return to an excited vibrational level instead of its initial ground state, producing a photon of lower frequency. The opposite case is also possible, an excited electron returns to a lower vibrational state while emitting a photon of larger energy. These two cases are known as Stokes and anti-Stokes shifts, respectively. Thermal occupation probabilities makes anti-Stokes shifts much less likely. The emitted photons are then collected by the spectrometer and analyzed according to their frequency. A display of photon counts versus frequency is provided to the user. Elastically scattered light is often filtered from the final results as it provides little information.

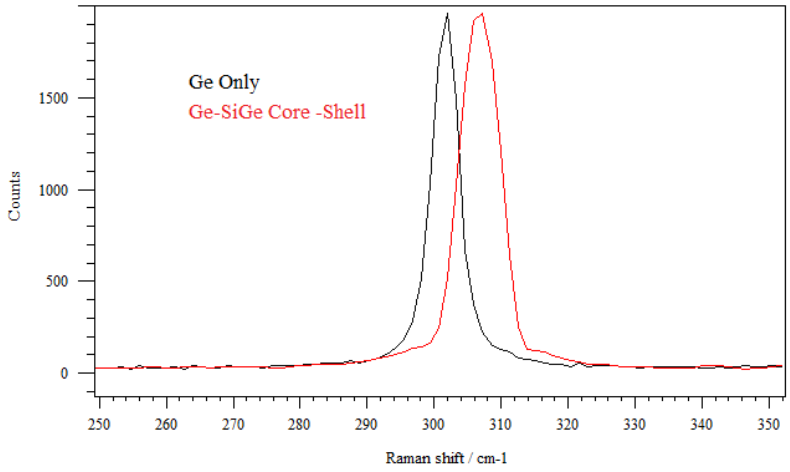

Figure 2.8. Raman spectra of a bare germanium (black) nanowire and a Ge-SiGe core-shell (red) with strained core. A peak shift of 5.0 cm^{-1} is clearly visible, indicating the possibility to measure strain in a core-shell structure.

Since a material's vibrational characteristics are directly linked to the bond angles and lengths present, Raman spectroscopy is sensitive to changes in crystal strain. In fact,

the use of this tool in strained silicon measurements has become routine for planar sample structures [22]. Strain measurements have also been performed on nanoscale Si/Ge structures, such as in the self assembled silicon germanium dots in a silicon matrix [23].

The sensitivity of Raman spectroscopy to detect strain from such small areas will allow for its implementation in core-shell nanowires. Initial measurements were taken for Ge-SiGe nanowires using a Renishaw InVia Raman microscope with a 532 nm excitation source, shown in Figure 2.8. Two samples were prepared: one using a bare germanium nanowire and the other, a strained core-shell structure. Both samples were dispersed in methanol on a patterned glass substrate to avoid possible spectral overlap with a silicon substrate. The Raman spectrum of the germanium nanowire, used as a control, is shown in black with the Ge-Ge peak located at 301.8 cm^{-1}. The core-shell nanowire spectrum, in red, shows the same peak now shifted to 306.9 cm^{-1}, indicting measurable strain. More work must be done to understand the effects of different strain components along with the role nanowire size plays in its Raman spectrum.

2.6 SUMMARY:

The need for an n-type device, complementary to the Ge-SiGe core-shell nanowire field-effect transistor, was discussed. This has so far eluded the Si/Ge material system, as unstrained band offsets are predominately in the valance band. However, with the application of strain, a type-II band alignment and the corresponding electron confinement has been realized in Si-SiGe heterostructures. The possibility of a similar situation appearing in core-shell nanowires was explored.

Strain distribution in a core-shell nanowire was calculated analytically, other possible methods were also introduced. The use of cylindrical coordinates in the solution lead to only two strain components in the final result: axial strain in the [111] direction, along with radial strain of an undefined orientation. Radial strain in both the core and the shell were shown to change very little with nanowire dimension. This component is tensile in nature for both regions, with the magnitude of the core's radial strain nearly vanishing. In contrast, axial strain was found to vary widely with dimension in either region. The core's axial strain was always tensile while that of the shell was at all times compressive. Cylindrical strain distributions were converted to Cartesian coordinates for the calculation of hydrostatic strain, an important parameter in shifted band structure models. Hydrostatic strain was found to be constant throughout the core and the shell.

The shift of the conduction band energy in the core and the shell were calculated with ***k•p*** theory and the analytic strain results; maximum band offset was found to be 200 meV for a Si-$Si_{0.2}Ge_{0.8}$ core-shell structure. For a more reasonable shell composition of $Si_{0.5}Ge_{0.5}$, an offset of 88 meV is predicted. Nanowire dimension was found to have a negligible effect on the calculated band offset.

Future work into strain engineering of core-shell nanowires was also presented. These structures will be grown by the vapor-liquid-solid mechanism in a UHV-CVD tool. Electrical characterization of the temperature dependant electron mobility will be used to determine if strain has, in fact, lead to core confinement. Raman spectroscopy will be used to directly measure the strain state in a given core-shell structure for comparison to

calculated values. Initial results were shown for a strained Ge-SiGe core-shell nanowire showing a strain-induced shift of the germanium peak, confirming the instrument's sensitivity to this technique.

Chapter 3: Modulation Doping of Core-Shell Nanowires

3.1 Introduction and Background:

High mobility materials, such as germanium and the III-V compound semiconductors, are of great interest to the device designer due to the performance enhancements they may allow. Intrinsic germanium possesses a low-field mobility well over twice that of silicon for both carrier types: 3900 $cm^2V^{-1}s^{-1}$ versus 1500 $cm^2V^{-1}s^{-1}$ for electrons and 1900 $cm^2V^{-1}s^{-1}$ versus 450 $cm^2V^{-1}s^{-1}$ for holes at room temperature. The electron mobility of gallium arsenide can approach 8000 $cm^2V^{-1}s^{-1}$ at room temperature, five times that of silicon. As with any semiconductor, however, these large bulk mobility values generally do not hold when fabricated into electronic devices. The influence of scattering from ionized dopants and surface states at the semiconductor-insulator interface often lead to mobility degradation. The effects of ionized impurity scattering, in particular, become more pronounced as impurity/dopant concentration rises. For electrons confined in a doped, two-dimensional quantum well, this inverse relationship has been shown to resemble [24]:

$$\frac{1}{\tau_c} \propto \int dz |F(q,z)|^2 N(z) \int_0^{\pi} d\theta (1 - cos\theta) \frac{1}{[q\varepsilon(q)]^2} \tag{3.1}$$

where τ_c is the electron relaxation time of a one-subband system due to the ionized impurity distribution $N(z)$, $F(q,z)$ is a measure of the electron wave function's overlap with charge centers, θ is the scattering angle, $q = 2\boldsymbol{k}\sin(\theta/2)$, and $\varepsilon(q)$ is the dielectric function.

Modulation doping was developed in the late 1970's as a way around this inherent

trade-off between doping density and mobility [25]. In this first demonstration, an AlGaAs/GaAs superlattice was grown in a molecular beam epitaxy (MBE) system. The structure was selectively doped with silicon only in the large band gap AlGaAs regions, leaving the small bandgap GaAs with only the background impurity concentration. Free electrons from the ionized donors are then spatially transferred and confined to the undoped GaAs conduction region. Two different doping profiles were used: one with dopants across the entire AlGaAs layer and one where only a portion of this region was doped, with an intrinsic spacer layer on either side. Another control sample used uniform doping throughout the entire layer sequence.

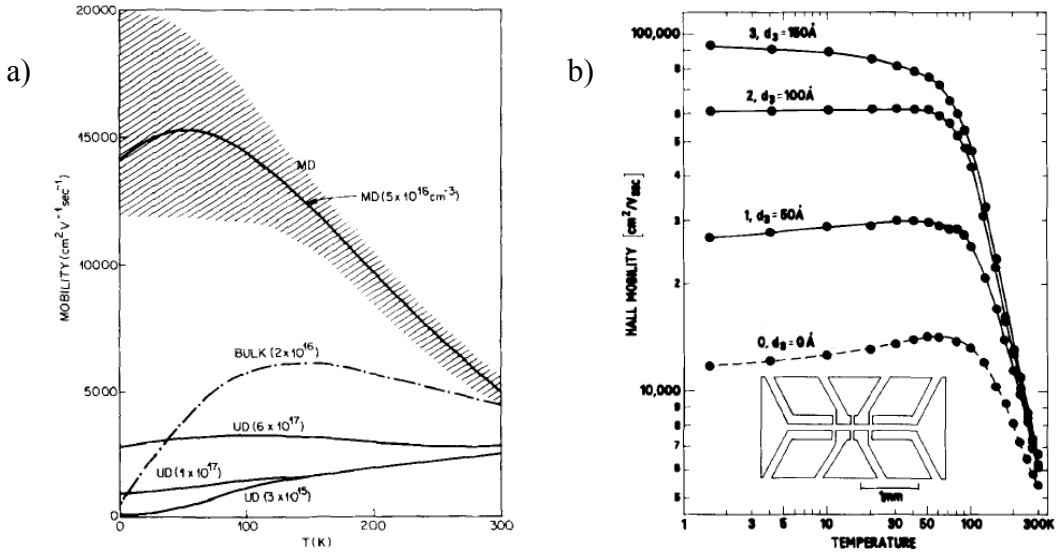

Figure 3.1: a) Hall mobility versus temperature for modulation doped (MD) and uniformly doped (UD) AlGaAs/GaAs superlattices of varying dopant density [25]. b) Hall mobility versus temperature for different undoped spacer layer thicknesses in a similar modulation doped structure [26].

The authors of [25] performed temperature-dependant Hall mobility measurements for samples of varying dopant profile and density, shown in Figure 3.1 a).

A clear enhancement in mobility is seen for the modulation doped devices, especially at low temperature. Crosshatched regions in the figure indicate the range of values obtained for different modulation doped samples, with and without undoped spacers. Uniformly doped samples show, depending on the impurity concentration present, either a constant or a reduced mobility at low temperature, indicating dominance of ionized impurity scattering. On the other hand, modulation doped samples show an increasing mobility as temperature is lowered from 300˚K to below 100˚K. This is indicative of a phonon limited scattering rate in that range. Below 60˚K, mobility begins to drop for even the modulation doped samples, probably due to the finite background impurity concentration of the GaAs layer.

The effect of undoped spacer layer thickness has been studied extensively for a number of different material systems, including the AlGaAs/GaAs structure from above [26]. As expected, the Hall mobility over the entire temperature range was shown to increase with each successive widening of spacer thickness, shown in Figure 3.1 b). As free electrons are separated farther from ionized dopants, the charged impurity scattering rate continually decreases, resulting in further mobility enhancement.

Modulation doping has also found use in the Si/Ge material system for both n- [7] [8] [27] and p-type [28] [29] [30] samples. Due to a strain-induced type-II band offset, electron and hole confinement now takes place in separate layers. The formation of a two-dimensional electron gas is accomplished through modulation doping of the germanium-rich barrier layer of the Si-SiGe heterostructure. Electrons are subsequently

transferred to the silicon transport layer. The opposite is true for modulation doping of a hole gas in a Ge-SiGe heterostructure: the silicon-rich layer now acts as a doped barrier and holes are confined into germanium. This behavior is in contrast to the more common type-I offset where both electrons and holes are confined into the same, smaller bandgap material.

The efficacy of this technique should not be limited to planar heterostructures or superlattices. Extension of modulation doping to germanium – silicon germanium core-shell nanowire heterostructures is an interesting opportunity. The combined vapor-liquid-solid and chemical vapor deposition method (Section 2.5.1) used in the production of core-shell nanowires, allows for radial variation in the shell's dopant density. Due to the significant valence band offset in this material system, holes should be efficiently transferred and confined to the core. The carrier concentration and drive current in a given device would increase, while also minimizing the mobility degradation associated with conventional doping. Careful optimization of dopant density and position, along with core/shell dimensions, is possible with the VLS/CVD growth method and is necessary in avoiding parallel, low-mobility conduction paths through the shell region.

The possibility of p-type modulation doping in germanium – silicon germanium core-shell nanowire heterostructures will be the topic of the remainder of this chapter. Section 3.2 will discuss the simulation of hole transfer from a boron doped shell to the intrinsic germanium core at different shell dimensions and dopant densities. An optimized set of parameters is determined based off these results. Details on the growth

and characterization of p-type modulation doped nanowires will be given in Sections 3.3 and 3.4, respectively. A possible extension of this project to n-type doping is discussed in Section 3.5.

3.2 Simulation of Carrier Transfer in Modulation Doped Core-Shell Nanowires:

The first stage in the design of a modulation doped Ge-SiGe core-shell nanowire was the simulation of core carrier concentration as a function of doping parameters. In any modulation doped structure, not all carriers are expected to be transferred to the undoped region, resulting in a parallel conduction path through the doped regions. In this particular case, the mobility of the parallel path is expected to be very low due to proximity to charged impurities and surface states, along with the intrinsically lower mobility of the silicon germanium shell as compared to germanium. For these reasons, the main figure of merit in this study was determined to be the ratio of confined holes in the core to the total number of holes in the structure. Maximization of this parameter, along with the undoped spacer layer thickness, should provide as large a drive current as possible without degrading mobility.

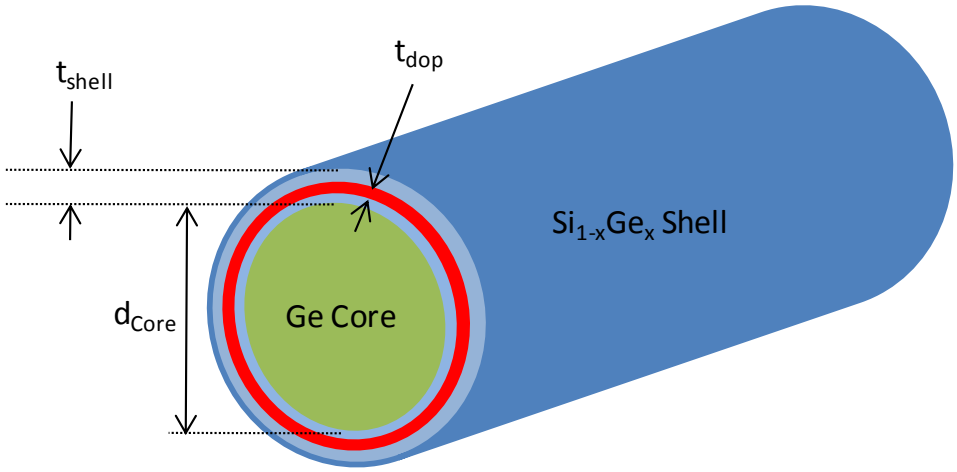

Figure 3.2: Three dimensional schematic of core-shell nanowire with modulation doped shell. Green and blue areas represent the core and shell, respectively. The boron doped region is shown in red, centered in the shell. Core and shell are assumed to have an intrinsic impurity concentration of 1 x 10^{10} cm^{-3}.

Finite element simulations were carried out using the Sentaurus Device software package from the Synopsys TCAD © suite of tools (version C-2009.06). A sample three dimensional device schematic is shown in Figure 3.2 for a Ge-$Si_{1-x}Ge_x$ core-shell nanowire with core diameter d_{core}, shell thickness t_{sh}, and boron doped region of thickness t_{dop}, centered in the shell. A shell composition of $Si_{0.4}Ge_{0.6}$ will be used mainly throughout this study and length of the simulated structure is fixed at 1.0 μm. The nanowire's cylindrical symmetry allowed for a two-dimensional solution to be used, minimizing the number of nodes required to model the structure. Using the "Cylindrical" command, Sentaurus automatically revolves a radial slice of this structure along its centerline to recreate the three dimensional structure. Background impurity concentration

in the undoped regions was assumed negligible, a value of $1x10^{10}$ cm^{-3} was used.

Solutions of hole distribution across this structure were found by self-consistent calculations using the Poisson, electron/hole continuity, and hole quantum potential equations. No gate bias was used in these tests. As seen in Figure 3.3 a) for a sample with $1x10^{18}$ cm^{-3} doping, hole distribution does not change with axial position, allowing use of one-dimensional radial slices to fully describe simulation results. A number of these slices are shown in Figure 3.3 b) for modulation doping densities between $1x10^{18}$ and $1x10^{20}$ cm^{-3}. It is clear that as doping density increases, hole density in the shell increases faster than that in the core due to incomplete spatial transfer. The simulated valence band profile is shown against radial position in Figure 3.3 c). Sentaurus' default value of 91.1 meV was assumed as the valence band offset between Ge and $Si_{0.4}Ge_{0.6}$.

Linear hole density was found through a discrete integration, in both the core and shell regions, of the data in Figure 3.3 b), taking into account the cylindrical symmetry of this structure. Simulations were done for nanowires with shell thicknesses of 5.0, 10, and 15 nm; the modulation doped region is 1.0 or 5.0 nm thick and is placed either at the center of the shell or at its outer edge. Germanium core radius was a constant 30 nm and shell composition remains $Si_{0.4}Ge_{0.6}$. Core hole density for these shell and doping combinations is given in Figure 3.4 a). Hole density rises with doping concentration to ~$5x10^{17}$ cm^{-3} (5.0 nm doping thickness) or $5x10^{18}$ cm^{-3} (1.0 nm doping thickness) where it begins to saturate. Below this value, nearly all carriers are confined to the core. For higher doping concentrations, however, any additional carriers spill over into the shell.

The similarity of curves with equivalent doped region thicknesses indicate that hole transfer is largely unaffected by other parameters (shell thickness, dopant position) as long as the doping density is chosen to be low enough to limit spill-over.

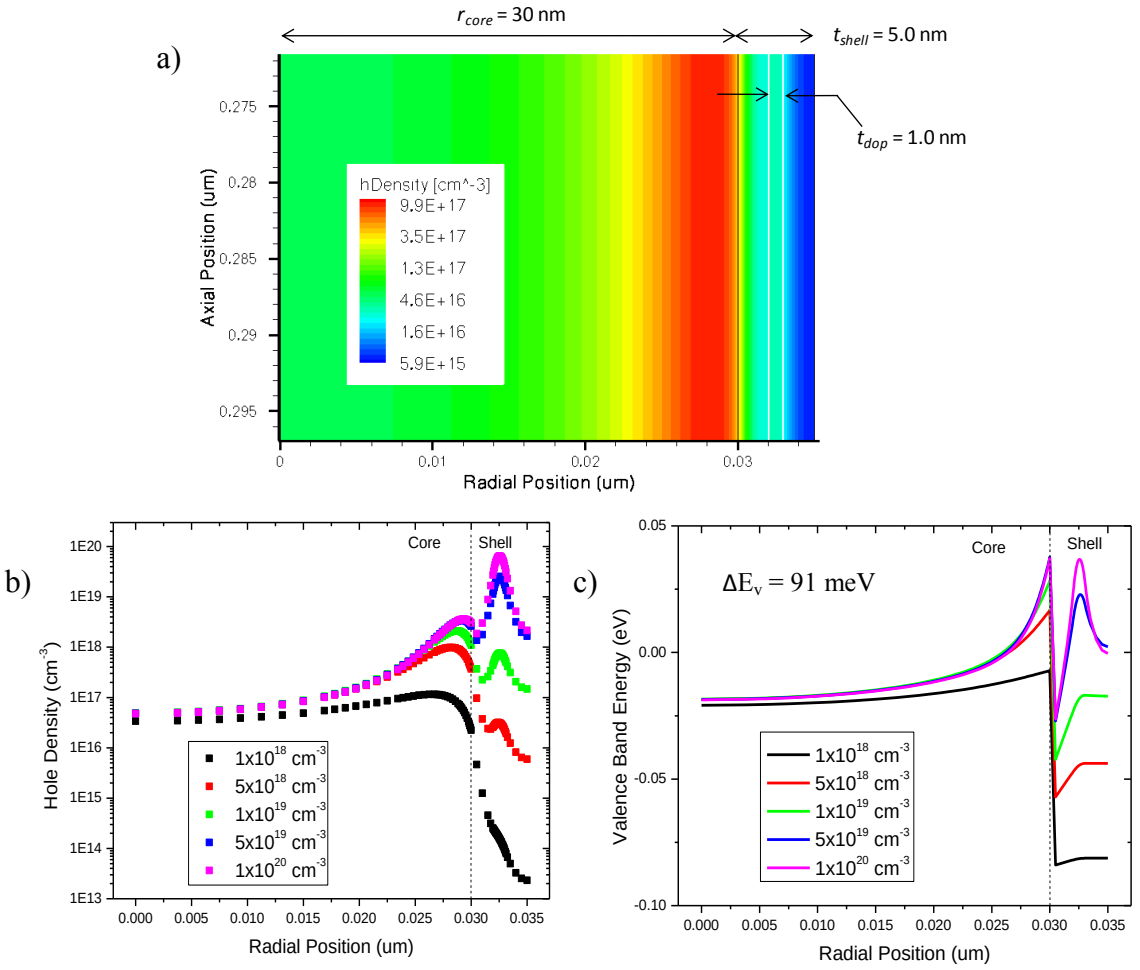

Figure 3.3: a) Hole density distribution in a modulation doped Ge-$Si_{0.4}Ge_{0.6}$ core-shell nanowire. Dopant density at the shell's center is $5x10^{18}$ cm^{-3}. Radial slice of b) hole density and c) valence band energy for five modulation doping densities between $1x10^{18}$ and $1x10^{20}$ cm^{-3}. Sample temperature is 77˚K in all.

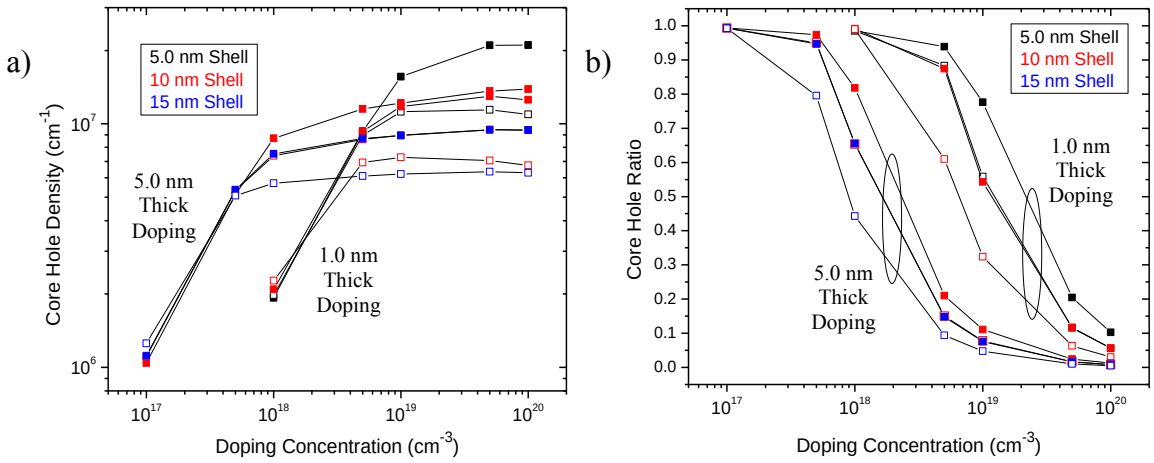

Figure 3.4: a) Hole density in the core and b) core hole ratio versus modulation doping density for nanowires of varying shell thickness, doped region thickness, and dopant position. All values are for a sample temperature of 77˚K. Filled (open) symbols correspond to a doped layer at the shell's center (edge).

The maximum hole density available in the core depends significantly on the undoped spacer layer thickness. Reducing the barrier thickness causes an increase of the built in electric field at the core/shell interface, effectively confining more carriers. This can be seen in the two cases of a 10 nm shell with 5.0 nm edge doping and a 15 nm shell with 5.0 nm center doping. Both have equivalent spacer thicknesses, leading to nearly identical hole densities at each doping level.

As expected, hole density in the core depends strongly on the shell's composition. Increasing silicon content creates a larger valence band offset between core and shell, allowing for a larger hole density before carrier spill over occurs. Moving from a $Si_{0.4}Ge_{0.6}$ shell to $Si_{0.6}Ge_{0.4}$ changed the (unstrained) valance band offset from 91.1 meV to 208 meV, producing a three-fold increase in maximum core hole density. The results of this study will focus exclusively on the lower silicon content shell due to the

possibility of strain-induced shell surface roughening in a highly lattice-mismatched interface [11].

As described earlier, the ratio of core hole density to total density was deemed to be the main figure of merit in this study; this data can be seen in Figure 3.4 b) for the same nanowire configurations as above. Similar to the case of core hole density, this ratio is shown to follow similar doping dependence for structures with the same doped layer thickness, shifted from each other by an order of magnitude in doping level. Below $1x10^{17}$ cm^{-3} (5.0 nm doped layer) or $1x10^{18}$ cm^{-3} (1.0 nm doped layer) hole transfer is nearly 100% efficient for all combinations tested. Above these values spill-over will occur and the ratio is now dependant on spacer layer thickness. Thin spacers act to amplify the core hole ratio at the expense of increased remote impurity scattering rate.

3.3 Design and Growth of Modulation Doped Core-Shell Nanowires:

Insight gained from the previous section was used in designing an optimum modulation doping scheme for experimental testing. Ultimately, core/shell dimensions and doping parameters will be used which maximize the core hole ratio of Figure 3.4 b), providing large carrier mobility while minimizing any parallel conduction paths in the shell.

Since carrier concentration in the core is not the first concern, doping concentration and doped layer thickness should be kept as small as possible. This will minimize hole occupation of the shell, reducing conduction through these low mobility states. Boron doping of SiGe had yet to be quantified in the chemical vapor deposition

(CVD) tool used for nanowire growth. A calibration run was performed by K. Varahramyan and myself using a (100) silicon wafer as substrate. After native oxide removal with hydrofluoric acid, a planar silicon germanium layer was grown by co-flowing 50 sccm silane (SiH_4, 100%) and 10 sccm germane (GeH_4, 20.8% in He). Diborane (B_2H_6, 100ppm in He), flowing at 10 sccm, provides p-type doping. Total growth time was 90 minutes at a temperature and pressure of 500˚C and 0.03 torr, both typical of silicon germanium nanowire shell conditions. This sample was then sent for analysis by secondary ion mass spectrometry (SIMS) at Cerium Labs (Austin, Texas). Depth profiling showed a boron doping concentration of roughly $6x10^{19}$ cm^{-3} in the silicon germanium layer. The same diborane flow rate and dilution, 10 sccm and 100ppm, will be used for actual nanowire growth. Two other samples will also be grown using 50 and 1.0 sccm diborane flow, providing a wide range of doping concentration.

Doped region thickness will be kept as thin as possible in order to maintain an acceptable ratio of core holes, even when large doping concentrations are used. The target thickness for this layer is 1.0 nm. However, this may end up larger in practice due to boron surface segregation during epitaxial shell growth.

A previous nanowire growth, NW63, was used as a base recipe for these modulation doped wires. This Si-SiGe core-shell nanowire features a 10 nm shell of roughly 40% silicon composition [31]. All growth parameters, with the exception of boron doping, were repeated by K. Varahramyan and I using the combined vapor-liquid-solid and chemical vapor deposition growth procedure introduced in Section 2.5.1. Gold

was first evaporated onto a (111) silicon wafer which was then annealed in the growth chamber at 500˚C under a hydrogen ambient. Germanium core growth was initiated at 1 torr chamber pressure and was increased to 2.5 torr after 15 minutes. Total core growth time was 65 minutes with 50 sccm germane (20.8% in He) flow at roughly 320˚C. Sample temperature was then increased to 500˚C and 10 sccm germane (20.8% in He), 50 sccm silane (100%) were introduced into the growth chamber at a total pressure of 0.04 torr for a total of 60 minutes. Diborane (100ppm in He) was employed at its desired flow rate during minutes 27 through 33 of growth, providing a 1.0 nm thick doping layer at the center of the shell. Table 3.1 lists diborane flow and other growth parameters for each modulation-doped nanowire series. Composition and thickness of the shell are assumed to be the same as that of the NW63 base recipe: 40% silicon and 10.0 nm. Cross sectional scanning electron microscope images of the as-grown wafer can be seen in Figure 3.5. Nanowires are shown to be predominately in the [111] direction and a maximum of 5.3 μm long.

NW Series	B_2H_6 Dopant Flow (sccm)	B_2H_6 Flow Time (min.)	Core Growth Temp. (˚C)	Core Growth Time (min.)	Core GeH_4 Flow (sccm)	Shell Growth Temp. (˚C)	Shell Growth Time (min.)	Shell GeH_4/SiH_4 Flow (sccm)
88	50	6	320	65	50	500	60	10/50
89	10	6	320	65	50	500	60	10/50
90	1	6	320	65	50	500	60	10/50
63	0	6	320	65	50	500	60	10/50

Table 3.1. Modulation-doped nanowire growth parameters. Only diborane dopant flow was changed between the three doped and one control sample. Diborane timing was constant as well: between minutes 27 and 33 of shell growth. Precursor dilution: GeH_4 – 20.8% in He, SiH_4 – 100%, B_2H_6 – 100ppm in He.

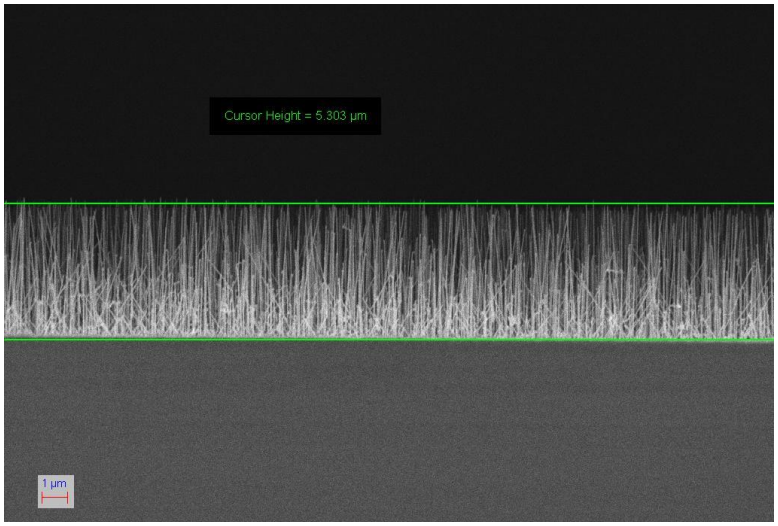

Figure 3.5: Scanning electron microscope image of an as-grown wafer of modulation doped core-shell nanowires, NW88, showing predominance of [111] growth and nanowire height of roughly 5.3 µm. Image provided by K. Varahramyan.

3.4 Electrical Characterization of Modulation Doped Core-Shell Nanowires:

Both back- and top-gated field-effect transistors were fabricated for each modulation doped nanowire growth. The four contact, back-gated device structures will be used to extract intrinsic hole mobility without seeing the effects of a finite metal to semiconductor contact resistance. Top-gate devices are used due to the large spread of threshold voltages between different modulation doped nanowires. Their increased gate capacitance allows for probing of each device at similar values of gate overdrive. Devices will be fabricated with ion implanted source/drain contact regions in order to obtain good ohmic contact between metal and semiconductor [32], particularly at reduced temperatures.

The back-gate substrate was fabricated first. A highly boron doped (100) silicon

wafer was thermally oxidized at 950˚C for two hours, resulting in 54 nm of SiO_2. An 8x8 array of alignment marks were then added by photolithography in order to aid in the location of suitable nanowires and to align metal contacts with precise control. AZ 5209 photoresist was spin-coated and prebaked for 120 s at 90˚C, followed by ultraviolet exposure in a Karl Suss MA6 mask aligner. Patterns were developed in AZ 726 and rinsed. An electron beam evaporator from CHA Industries was used to deposit 5.0 nm of titanium followed by 45 nm of gold. Liftoff in acetone was done to complete the process. For back-gate samples using ion implantation of the source and drain, much finer alignment marks are needed than can be provided by photolithography; in these cases extra alignment marks were added by electron beam lithography (EBL). Poly(methyl methacrylate) (PMMA) was spun on the sample and baked at 180˚C for three minutes. EBL exposures were done in a Raith 50 pattern generator. The sample is then developed in a 1:3 solution of MIBK:IPA for 60 s. Metal deposition and liftoff was done through the same procedure as above.

Nanowires were harvested from the growth substrate by sonication in ethanol for 10- 12 s. This solution was deposited onto a patterned back-gate substrate heated to 55˚C, resulting in a random distribution of nanowires across the sample's surface. Scanning electron microscope (SEM) imaging was done in a Zeiss Neon 40 to locate nanowires to be used for devices; their location was recorded in relation to nearby alignment marks.

After imaging, top-gate devices were etched of their native oxide by two consecutive cycles of 1:50 HF(49%):H_2O for 15 s, followed by rinsing in DI water. All

samples were immediately loaded into an atomic layer deposition (ALD) system set to 250˚C. A bare, 3 mΩ-cm p-type (100) silicon control wafer was also included for oxide thickness and capacitance measurements. Al_2O_3 top-gate dielectric was deposited by 60 cycles of alternating Trimethylaluminium (TMA) and water pulses, resulting in a thickness of 8.35 nm. Capacitance-voltage measurements of MOS capacitors patterned and deposited on the control sample indicate an accumulation capacitance of 9.18 x 10^{-7} Fcm^{-2}, leading to an Al_2O_3 dielectric constant of κ = 8.7. Gate patterns were applied through the standard EBL recipe listed above, followed by sputter deposition of TaN at 1.1 kW for 2.5 minutes. After lift-off, devices were etched of Al_2O_3 in the source/drain regions by 40 s in 1:40 HF(49%):H_2O. The TaN gate was used as both an etch and ion implantation mask.

Back-gate samples require the formation of an implant window to selectively dope only the areas to be covered with metal contacts. The standard EBL procedure was again used for these windows. All samples were then sent to Core Systems (Sunnyvale, CA) for boron implantation at 3 KeV with a $1x10^{15}$ cm^{-2} dose. PMMA was stripped from the back-gate samples with acetone, followed by a rapid-thermal activation anneal at 500˚C for 5 minutes.

Both back- and top-gate samples were patterned with EBL for metal contacts. 80 nm of nickel was deposited, with lift-off done as before. Six individual contacts were provided to each back-gate nanowire device, with spacing between the inner electrodes varying from 260 nm to 1 μm. This structure allows for four-point measurement of up to

three sets of contacts for each nanowire. Top-gate devices were designed with equal source/drain extension lengths of 500 nm to create a roughly constant contact resistance between devices. Devices of gate lengths between 250 nm and 1.5 μm were fabricated. The completed device structures can be seen in Figures 3.6 a) – c).

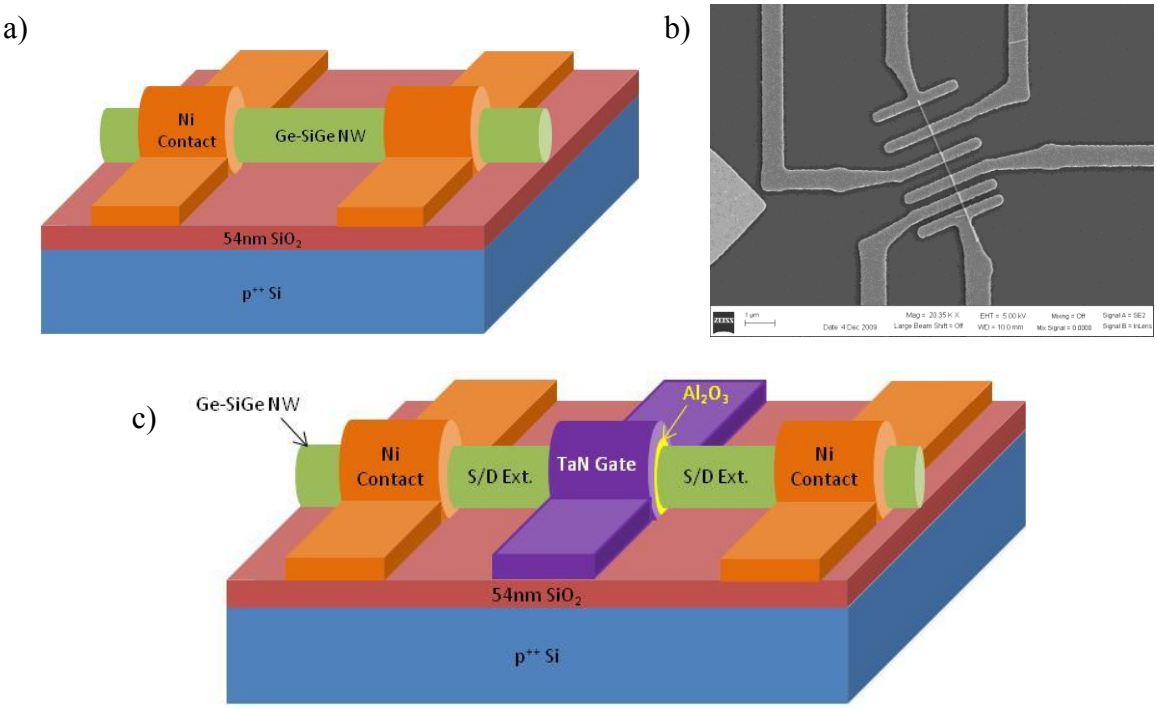

Figure 3.6: a) Three dimensional drawing and b) high magnification SEM image of back-gate device structure. Areas under Ni contacts are highly boron doped. c) Three dimensional drawing of top-gate device. Source/drain extensions are 500 nm for all devices. Nanowire is highly boron doped outside of gate region.

Electrical measurements were first performed on each back-gate sample in a Lakeshore Cryogenics probe station using an Agilent 4156C Semiconductor Parameter Analyzer. Outer contacts were used as a current source/drain and voltage across the inner electrodes were monitored using high-impedance inputs to the parameter analyzer. This

measurement configuration removes any effects of metal-semiconductor contact resistance as no current can flow to/from the inner contacts. Back-gate dependant output characteristics were measured at temperatures between 77˚K and 300˚K for each series of modulation doped nanowire. Figure 3.7 a) shows a typical room temperature four-point I_D-V_D curve for a 600 nm NW90 device with ion implanted contacts. A large positive threshold voltage was seen for all modulation-doped samples, indicating depletion-mode operation.

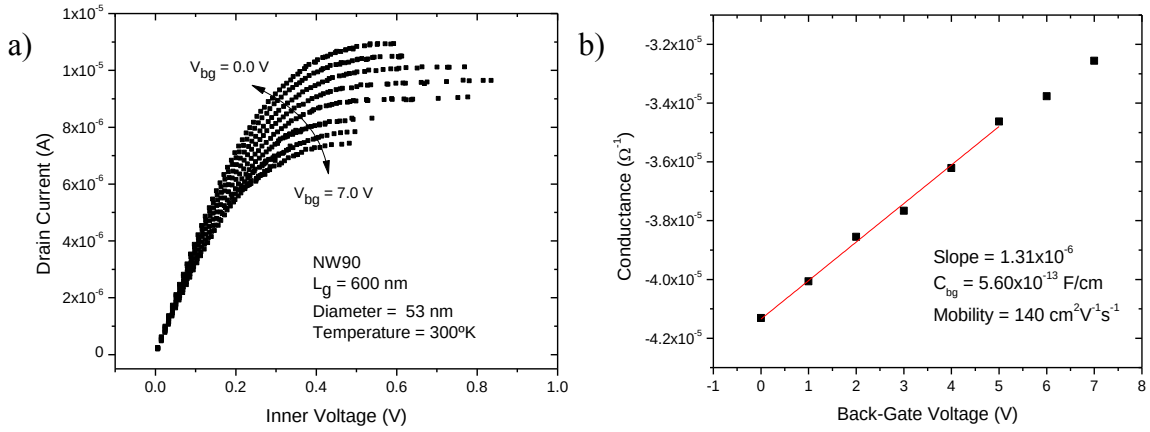

Figure 3.7: a) Room temperature, four-point output characteristics of a 600 nm channel length back-gate device using NW90 and ion implanted contacts. Inner voltage is the magnitude of the voltage drop between inner contacts. b) Low-field conductance versus back-gate voltage for the same device as in a). Slope of conductance is $1.31\text{x}10^{-6}$ $\Omega^{-1}\text{V}^{-1}$, corresponding to a mobility of 140 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$.

Low-field hole mobility can now be extracted from output characteristics through differentiation of the standard linear region MOSFET equation:

$$G_{ch} = \frac{1}{R_{ch}} = \frac{\mu_p C_{bg}\left(V_{bg} - V_{th}\right)}{L_{ch}} \tag{3.2}$$

$$\mu_p = \frac{dG_{ch}}{dV_{bg}} L_{ch} C_{bg}^{-1} \tag{3.3}$$

where G_{ch} is channel conductance at low drain bias and C_{bg} is the back-gate oxide capacitance per unit length. Figure 3.7 b) shows the extraction of dG_{ch}/dV_{bg} from gate dependant conductance data for the same device whose *I-V* characteristics are shown in Figure 3.7 a). Generally, a portion of the back-gate voltage range between -2.0 V and +5.0 V is used for linear data fitting. Back-gate capacitance is found by simulation of the gate-dependant hole concentration in Sentaurus Device: $C_{bg} = -e(dp/dV_{bg})$. Values of capacitance for nanowires of 30 to 60 nm diameter are shown in Figure 3.8. For the example device of Figure 3.7, $C_{bg} = 5.6 \times 10^{-13}$ Fcm^{-1} and the conductance slope is 1.31 x 10^{-6} Ω^{-1}V^{-1}. These values lead to a room temperature effective mobility of 140 cm^{2}V^{-1}s^{-1}.

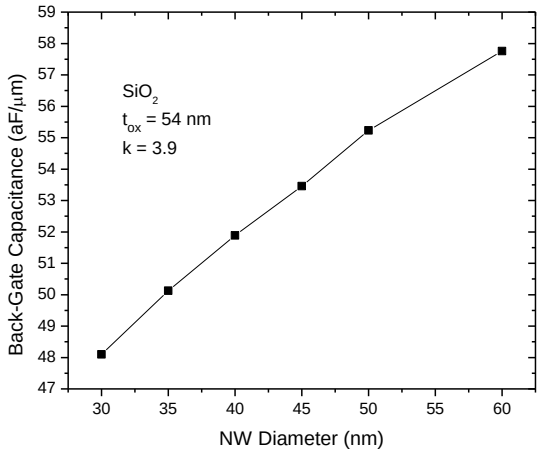

Figure 3.8. Simulated back-gate capacitance versus diameter for a Ge-Si0.4Ge0.6 core-shell nanowire. Gate dependant hole density was simulated in Sentaurus Device.

Low temperature hole mobility for the three series of back-gate, modulation doped nanowires with ion implanted contacts is shown in Figure 3.9. The three highest

mobility devices of each sample (filled symbols) are displayed, along with the sample's average mobility at each temperature point (open, connected symbols). Shaded regions have been added to help guide the eye. A total of 12, 9, and 7 devices were measured on sample NW88, NW89, and NW90, respectively.

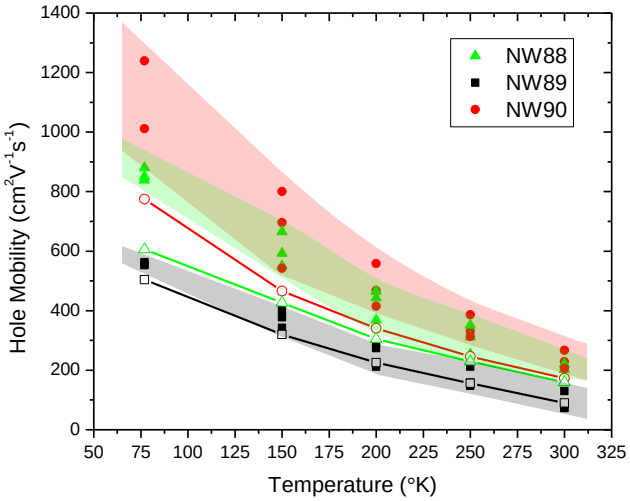

Figure 3.9: Low temperature hole mobility for three series of back-gate modulation doped nanowires with ion implanted contact regions. NW88 was doped the heaviest (50 sccm diborane flow) and NW90 the lightest (1 sccm). Open, connected symbols indicate average sample mobility at each temperature point.

As expected, the lightest doped nanowire, NW90, has the largest mobility across the entire temperature range, with average values of 173 and 775 $cm^2V^{-1}s^{-1}$ at 300 and 77˚K, respectively. Moving to the intermediately doped sample, NW89, results in a large reduction in mobility: the average value at room temperature is now 90.3 $cm^2V^{-1}s^{-1}$, increasing to 504 $cm^2V^{-1}s^{-1}$ at 77˚K. These values are consistent with the observations of Section 3.2. Increased modulation doping concentration will eventually cause a spill-over of holes from the core resulting in a significant conduction path through the shell. This

parallel path is of inherently low mobility due to the proximity of ionized dopants and surface states, along with the intrinsically low hole mobility of silicon germanium as compared to germanium. This trend, however, does not seem to hold for the results of NW88, the heaviest doped nanowire. Mobility values are between those of the previous samples, with averages reaching 160 and 606 $cm^2V^{-1}s^{-1}$ at 300 and 77˚K, respectively.

In Figure 3.10, mobility is shown as a function of each device's extrapolated threshold voltage. The fixed, charged impurity concentration was extracted from room temperature threshold voltage data by assuming that this value is proportional to the carrier concentration at zero gate bias. In order to provide a fixed relationship between threshold voltage and impurity concentration in the top axis of Figure 3.10, an average back-gate capacitance and nanowire diameter were used. The average impurity concentration of each sample was found to be 7.35 x 10^{19}, 2.56 x 10^{20}, and 8.26 x 10^{19} cm^{-3} for NW88, NW89, and NW90, respectively, while the extremes were 4.37 x 10^{19} (NW90) and 3.40 x 10^{20} cm^{-3} (NW89). The observed trend of increasing mobility with decreasing threshold voltage provides further insight into the results of Figure 3.9. Devices with large impurity concentration, NW89 in particular, suffer from increased charged impurity scattering, indicating that hole conduction is mainly through the shell at the gate biases measured.

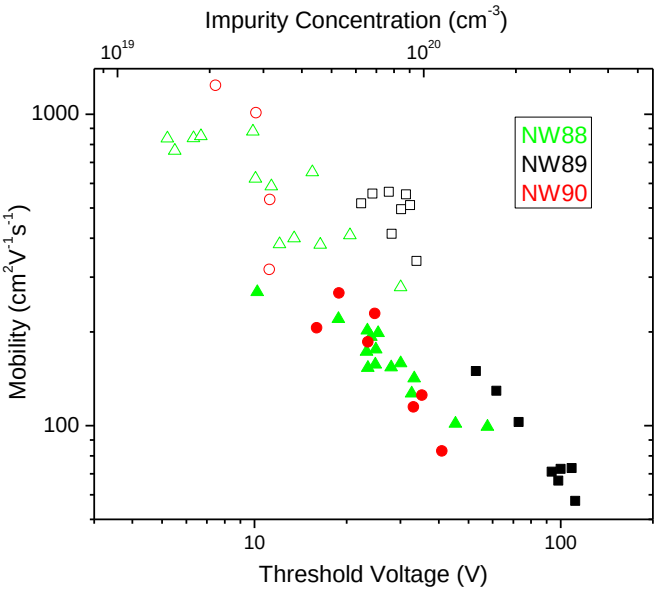

Figure 3.10: Mobility of back-gate modulation doped nanowires shown as a function of device threshold voltage (bottom axis) and fixed impurity concentration (top axis). Filled (open) symbols represent room temperature (77˚K) data.

The large sample-to-sample and device-to-device variations in threshold voltage, however, may obscure the mobility results of Figures 3.9 and 3.10. The method of mobility extraction employed here relies on the linear fitting of device conductance versus gate voltage at low drain bias. This data fitting should ideally be done at a constant range of gate overdrive voltages, V_{od}, to allow for a true comparison of mobility. As gate voltage is increased above threshold, a sharp rise in mobility is expected due to more efficient carrier screening of charge centers at the semiconductor-oxide interface. Further increasing gate overdrive voltage leads to a leveling off and eventual decay of mobility; a result of surface roughness scattering at high transverse electric field. The low capacitance of the back-gate structure has lead to a large spread in threshold voltage between samples and the inability to probe these devices nearer to their threshold.

Top-gate devices, therefore, should be used to verify the previous mobility data of these modulation-doped nanowire heterostructures. Their simulated capacitance, shown in Figure 3.11, is over 20 times that of back-gate structures, allowing for probing at, or near, their threshold voltage and extraction of their peak mobility. The simulation and extraction of top-gate capacitance is analogous to the case of back-gate devices described above. Current-voltage (*I-V*) measurements were performed on three modulation doped samples in a Lakeshore Cryogenics probe station using an Agilent 4156C Semiconductor Parameter Analyzer. Figure 3.12 shows the typical room temperature characteristics of a NW90 device with 610 nm gate length and 35 nm diameter. Threshold voltage of this particular device was measured to be 2.74 V.

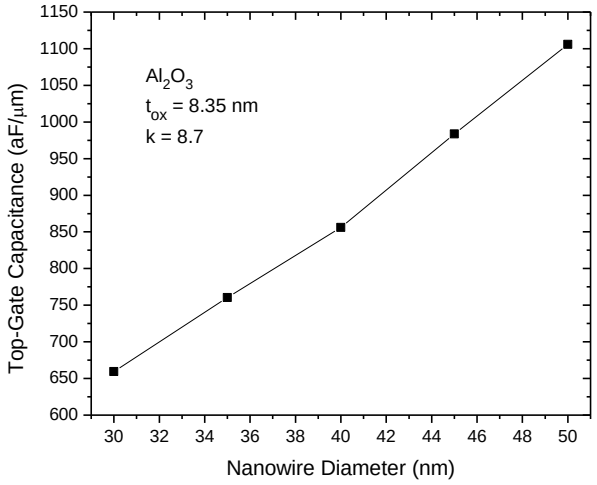

Figure 3.11. Simulated top-gate capacitance for a Ge-$Si_{0.4}Ge_{0.6}$ core-shell nanowire of varying outer diameter. Gate dependant hole density was simulated in Sentaurus Device.

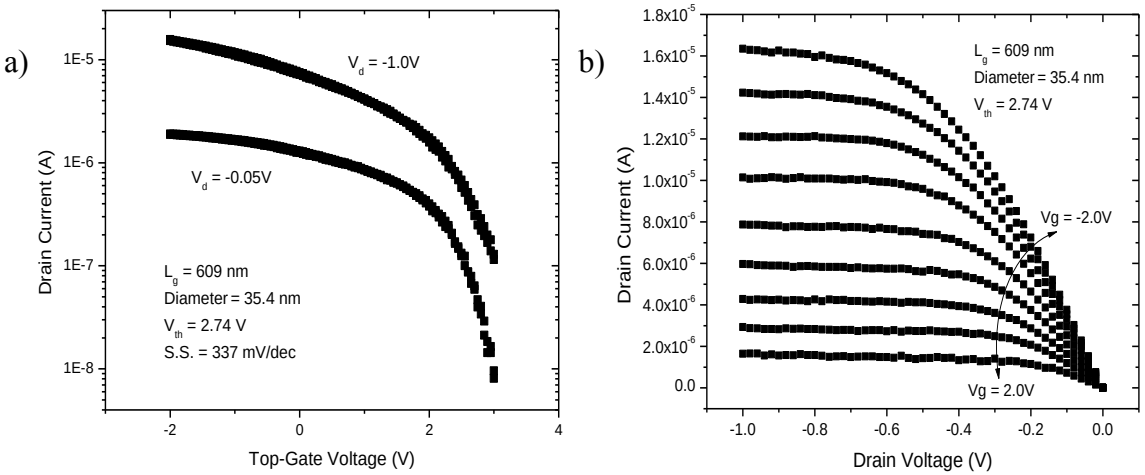

Figure 3.12. a) Transfer (I_d-V_g) and b) output (I_d-V_d) characteristics of top-gated NW90 device with 610 nm gate length, 35 nm diameter. Measured threshold voltage and subthreshold swing are 2.74 V and 337 mV/dec, respectively.

The two-point contact structure of these devices requires the extraction of extrinsic device resistance through linear extrapolation of gate length dependant channel resistance at constant gate overdrive values [33]. Lines for different gate overdrive voltages intersect at one common point, corresponding to the external source/drain resistance, R_{sd} (the sum of contact, doped source/drain extension, and other measurement circuit resistances), and channel length reduction, ΔL (the difference between the geometric gate length and the effective channel length). Figure 3.13 shows the extraction of the extrinsic source/drain resistance, R_{sd} = 15.3 KΩ, and channel length reduction, ΔL = -57.7 nm, for data from NW89 at room temperature. Source/drain resistance for the other modulation doped samples at room temperature and 77˚K are given in Table 3.2.

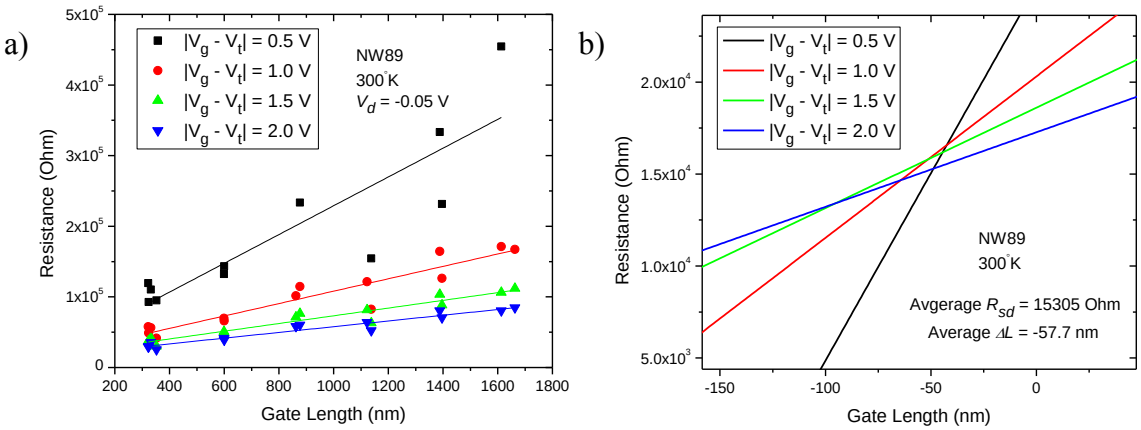

Figure 3.13. a) Channel resistance of top-gate NW89 device as a function of gate length for gate overdrive voltages between 0.5 and 2.0 V. Resistance was measured at a constant drain voltage of -0.05 V. b) Crossover of the linear fit to data showing average values of V_{sd} = 15.3 KΩ and ΔL = -57.7 nm.

The low-field, intrinsic mobility may now be calculated for each device from their measured transfer characteristics (I_d - V_g) by the following equation:

$$\mu = \frac{L_g}{R_{ch} C_{ox} \left(V_t - V_g - 0.5 V_d\right)} \tag{3.4}$$

where R_{ch} is the difference between the measured device resistance at V_d = -0.05 V and the extracted source drain resistance for the sample under consideration. At 77˚K, mobility shows the typical dependence on gate overdrive voltage: a steep initial rise as threshold is surpassed, caused by increasingly efficient carrier screening of charged traps, followed by a steady decline due enhanced surface roughness scattering at large transverse electric fields. Typical low-temperature mobility curves are shown in Figure 3.14 a) for a NW88 device with L_g = 1050 nm and a 43 nm diameter (black squares) and a NW90 device with L_g = 1140 nm and a 36 nm diameter. These devices show peak mobility of 789 and 944 $cm^2V^{-1}s^{-1}$ at gate overdrive voltages of 0.21 and 0.15 V,

respectively. A smaller, secondary mobility peak at larger gate overdrive voltage is also seen for most of the modulation doped devices. However, at low temperature its magnitude is much smaller than the initial peak.

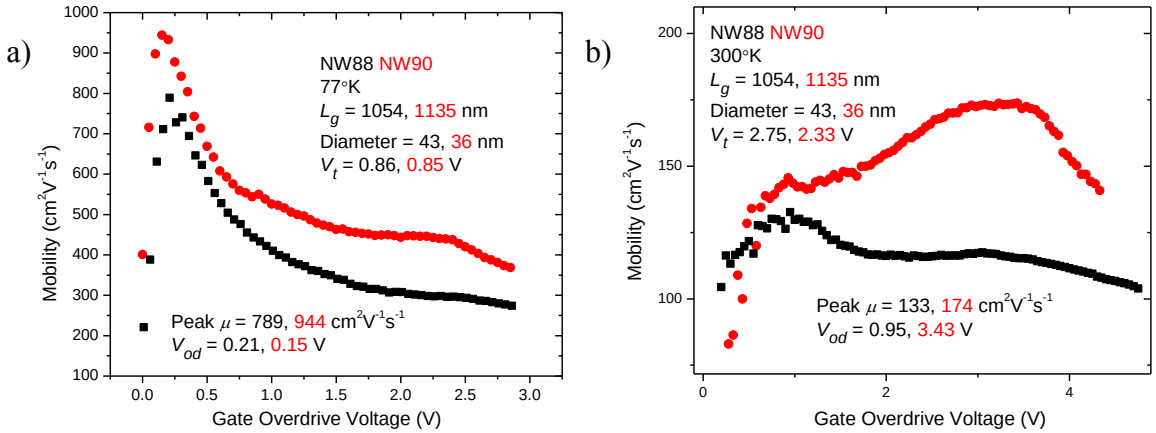

Figure 3.14. Mobility versus gate overdrive voltage for typical top-gate NW88 (black) and NW90 (red) devices at a) 77˚K and b) 300˚K.

Figure 3.14 b) shows the room temperature mobility data for the same devices as in Figure 3.14 a). In this case, peak mobility reduces to 133 (NW88) and 174 cm^{2}V^{-1}s^{-1} (NW90) at V_{od} = 0.95 (NW88) and 3.43 V (NW90). The double-peak mobility structure also becomes much more pronounced than at low temperature. Overall, the NW88 sample has roughly equal probability of a given device reaching its global mobility maximum in the first or second peak, while the other samples, NW89 and NW90, most always reach their highest mobility at larger gate overdrive voltages.

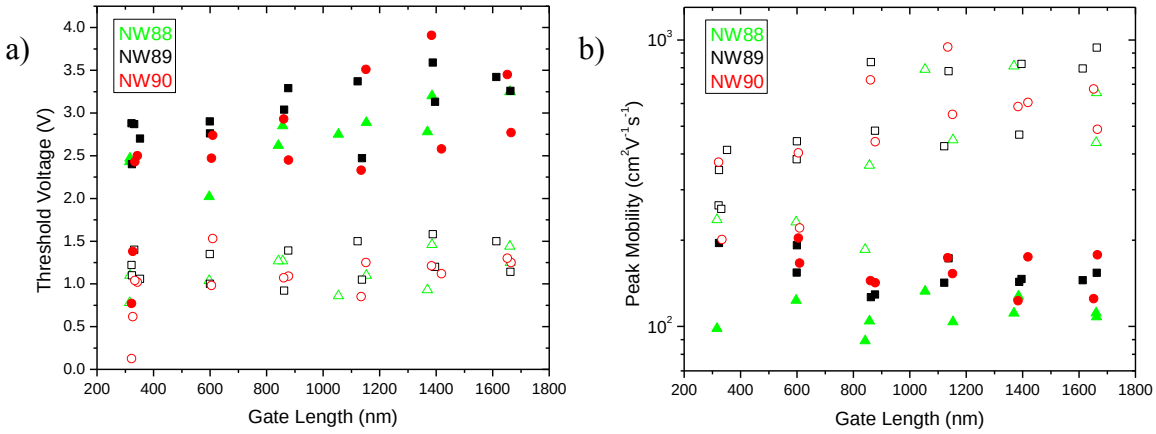

Figure 3.15. Threshold voltage and peak mobility as a function of gate length for three top-gate modulation doped device samples: NW88 (green), NW89 (black), and NW90 (red). Filled symbols represent room temperature data, open symbols are for data at 77˚K.

NW Series	R_{sd} (KΩ) 300˚K	R_{sd} (KΩ) 77˚K	Avg. V_t (V) 300˚K	Avg. V_t (V) 77˚K	Avg. Peak Mobility ($cm^2V^{-1}s^{-1}$) 300˚K	Avg. Peak Mobility ($cm^2V^{-1}s^{-1}$) 77˚K
88	11.1	5.27	2.77	1.14	111	462
89	15.3	6.04	3.01	1.24	155	547
90	16.2	6.04	2.59	1.03	158	547

Table 3.2. Source/drain series resistance, R_{sd}, average threshold voltage, V_t, and average peak mobility values for each sample of top-gated modulation doped nanowire devices at room temperature and 77˚K.

A comparison of the room temperature (filled symbol) and 77˚K (open symbol) threshold voltage and peak mobility values of the three modulation doped nanowire samples is given in Figures 3.15 a) and b), along with their average values in Table 3.2. Average room temperature V_t increased from 2.77 V to 3.01 V when moving from NW88 to NW89. NW90, as expected, does show the lowest average threshold voltage of the three samples, 2.59 V. Results at low temperature were qualitatively similar: the average threshold voltage of NW89 was still the largest, with a value of 1.24 V. Observation of a

large threshold voltage in NW89 is also consistent with the results from back-gated devices. Overall, the threshold voltages of these samples show only a weak correlation with growth conditions, compared to variations within an individual sample. This large disparity may be due to sample-to-sample variability in dopant incorporation during shell growth or to differences in oxide charge trapping between samples.

Peak mobility of these samples were also seen to be weakly dependent on growth conditions, although a slight upward shift can be seen in the NW89 and NW90 samples. Average values of peak mobility for NW88, NW89, and NW90 are 462, 547, and 547 $cm^2V^{-1}s^{-1}$ at 77˚K and 111, 155, and 158 $cm^2V^{-1}s^{-1}$ at 300˚K, respectively.

To further investigate the mobility of these modulation doped devices, their drain currents at constant gate overdrive voltage (2.0 V) and drain bias (-1.0 V) were compared. The use of constant gate overdrive voltage in this evaluation factors out the effects of threshold voltage shift due to doping and, therefore, drive current should depend mainly on carrier mobility at the given carrier density. To account for varying nanowire diameter, drive current was normalized to the diameter of each device. The data of Figure 3.16 mirrors that of Figures 3.15: the nanowire growth condition had little effect on the measured drive current, probably due to a large trapped charge density in the gate oxide. Again, only a slight increase in drive current is seen moving from NW88 to NW89. Further decreasing the doping concentration produces little benefit.

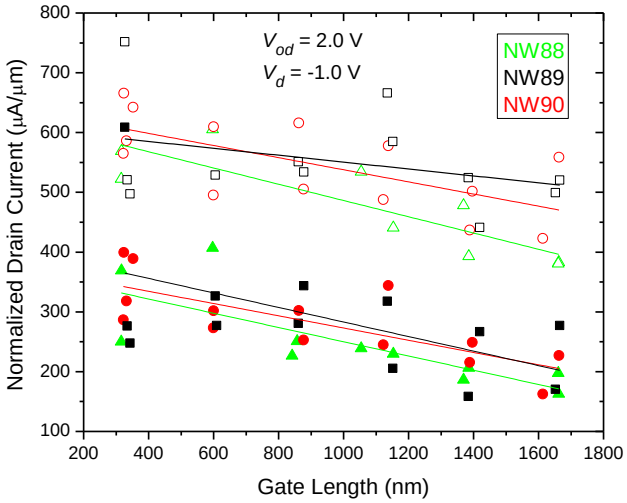

Figure 3.16. Normalized drain current of top-gate modulation doped devices at a constant overdrive voltage of 2.0 V and drain bias of -1.0 V. Filled (open) symbols indicate data at 300˚K (77˚K). Linear fit added to guide the eye.

Due to the large variability in threshold voltage, peak mobility, and drive current between devices of the same sample, there is uncertainty in the actual doping concentration of a given nanowire. Similar to the case of back-gate devices, the measured threshold voltage of an individual top-gated device is a better estimate of its fixed impurity concentration than its growth conditions. The peak mobility versus threshold voltage data of Figure 3.17 confirms an increasing mobility with decreasing V_t, particularly at room-temperature. These results seem to indicate that hole conduction through the shell is significant, even in the lightly doped devices (determined by low threshold) at the point of peak mobility. A flat mobility-V_t curve is expected in the lower threshold range if holes were strongly confined to the core. In that case, the ionized impurity scattering rate of Eq. (3.1) would reduce to that of remote ionized impurity scattering and an increase in doping density would not degrade carrier mobility.

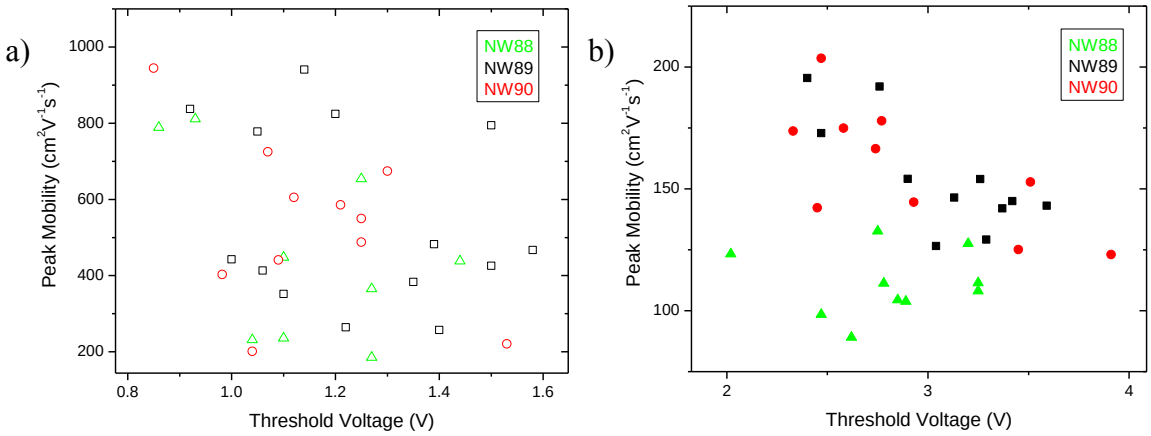

Figure 3.17. a) 77˚K and b) room temperature peak mobility of top-gate modulation doped core-shell NWFETs as a function of threshold voltage.

3.5 FUTURE WORK:

The design of Si-SiGe core-shell nanowire heterostructures for the confinement of electrons was in the main topic of Chapter Two. Mechanical strain was calculated for the core-shell structure and ***k·p*** deformation potential theory was applied in order to determine the conduction band offset at the core/shell interface. It was found that an acceptably large band offset is possible in nanowires of reasonable shell composition, allowing for electron confinement to the silicon core. Due to this confinement effect, the modulation doping technique could also be extended to these n-type devices. This would aid the experimental characterization of such a device through observation of the electron mobility evolution with temperature and doping concentration/position. If conduction was primarily through the core, we would expect increasing mobility at temperatures well below 77˚K and larger mobility when thicker undoped spacer layers are utilized. The growth of modulation doped Si-SiGe core-shell nanowires would be accomplished similar to the p-type devices presented here: a dopant precursor (likely phosphine, PH_3)

would be introduced for only a short time during CVD growth of the shell. These new nanowires would also be characterized in much the same way as the p-type devices: through the fabrication of back- and/or top-gated NWFETs, followed by current-voltage measurements at reduced temperatures.

3.6 SUMMARY:

Modulation doping is a method of providing free carriers to a material without the traditional mobility degradation associated with doping. Electrons or holes are separated from ionized dopants through real space transfer across a semiconductor heterostructure. This separation reduces the rate of ionized impurity scattering, leading to mobility enhancement. This enhancement is particularly significant at low temperature due to the diminishing effects of phonon scattering. Both n- and p-type modulation doping has been demonstrated in III-V and Si/Ge based planar structures. The potential for modulation doping of core-shell nanowires was discussed.

Simulations of hole density across a modulation doped Ge-SiGe core-shell nanowire structure were done with an eye towards maximization of the percentage of total holes which are confined to the core. Shell thickness, doping concentration, doped layer thickness, and doped layer position were all used as parameters in these simulations. It was found that this ratio of interest is most dependent on the total number of dopants present, i.e. doping concentration and doped layer thickness. Once a certain threshold is reached, each additional hole would spill out of the core and be conducted in a low mobility path through the shell.

Three modulation doped core-shell nanowire samples were grown, each using a different doping concentration. Both back- and top-gated field-effect transistors were fabricated and low temperature measurements were done in order to calculate hole mobility. An extremely large spread in threshold voltage between back-gate samples meant that devices could not be probed at equivalent gate overdrive voltages, leading to ambiguities in the measured back-gate mobility. Higher capacitance top-gate devices allowed for probing at, or near, threshold in all cases. It was found that device to device variation in top-gate threshold voltage and mobility was generally larger than the changes seen between samples of different growth conditions, indicating uncertainty in the true doping density in the shell. Therefore, threshold voltage is a better gauge of the actual doping density within a given device. The peak mobility of all samples show an increasing trend with decreasing threshold voltage, indicating that conduction, even at the point of peak mobility, is mainly through the shell.

An extension of the work in Chapter Two was proposed. Modulation doping would aid in the characterization of n-type Si-SiGe core-shell nanowire heterostructures through observation of the evolution of carrier mobility with changes in temperature and doping parameters, such as concentration and spacer layer thickness.

Chapter 4: Conclusion

The semiconductor industry has traditionally been built around the ever increasing data storage and computing power afforded to it by the scaling of individual MOSFET devices. Formerly, these improvements were limited only by the means of integrated circuit production, particularly the minimum available resolution of photolithography processes. There are now, however, a number of fundamental restrictions to further scaling, leading to the non-ideal electrical characteristics called short channel effects.

Three-dimensional device structures, and the semiconducting nanowire in particular, have been recognized as possible alternatives to traditional CMOS architecture. The improved electrostatic control of the gate-all-around geometry leads to a reduction in short channel effects over their planar counterparts. Carrier mobility has also shown to benefit from the incorporation of higher mobility materials, such as germanium, along with the possibility of radial band engineering using core-shell heterostructures. This thesis discusses two such methods of enhancing the carrier mobility of core-shell nanowires.

We have evaluated the prospect of electron confinement in a strained Si-$Si_{1-x}Ge_x$ core-shell nanowire heterostructure. Strain distribution was calculated analytically for structures with various dimension combinations and shell composition. Shifts of both the Δ and L conduction band valleys were found using $\boldsymbol{k \cdot p}$ deformation potential theory, along with the strain-induced coordinate system transformation of Pikus-Bir. We found that radial strain in the silicon core nearly vanishes when shell thickness is less than 10

nm, leading to only negligible valley splitting in this region. Band splitting in the shell, however, was shown to be much larger, over 200 meV, due to its increased radial strain magnitude. The cylindrical geometry leads to a non-uniform angular distribution of strained band energies in the shell. Conduction band offset was, therefore, calculated using the point of minimum energy in the shell. We find that a positive conduction band offset of up to 200 meV is possible in a Si-$Si_{0.2}Ge_{0.8}$ core-shell nanowire. The ultimate band offset was seen to be insensitive to changes in core/shell dimensions.

We also present here a study of p-type modulation doping in Ge-$Si_{0.4}Ge_{0.6}$ core-shell nanowires. Finite-element simulations of hole density in this structure were done in order to provide insight into desired doping parameters. The growth of modulation doped core-shell nanowires was accomplished through a two-part, vapor-liquid-solid and chemical vapor deposition, process. A 1.0 nm thick boron-doped ring was included at the center of the shell. We have grown three such samples, each using a different diborane gas flow rate. Estimated modulation doping concentration of these nanowires ranged from 4.37×10^{19} to 3.40×10^{20} cm^{-3}. Each sample was characterized through low-temperate current-voltage measurements of both back- and top-gated field-effect transistors. We found a large range of threshold voltage and mobility for devices of a given sample, indicating variations in dopant density or in the density of fixed charges in the oxide layer. Therefore, we believe the threshold voltage of each device is a better gauge of fixed impurity concentration than its growth condition. The room-temperature mobility of each sample was found to follow a consistently increasing trend with decreasing

threshold voltage, indicating that carrier mobility is limited by ionized impurity scattering from a combination of boron dopants in the shell and fixed charges in the gate oxide.

References

1. R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, A. R. LeBlanc, IEEE J. Solid-State Cir. **9**, 256 (1974).

2. Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, S.-H. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H.-J. C. Wann, S. J. Wind, H.-S. Wong, Proc. IEEE **85**, 486 (1997).

3. C. P. Auth, J. D. Plummer, IEEE Elect. Dev. Lett. **18**, 74 (1997).

4. R. People, J. C. Bean, Appl. Phys. Lett. **48**, 538 (1986).

5. W. Lu, J. Xiang, B. P. Timko, Y. Wu, C. M. Lieber, Proc. Natl. Acad. Sci. **102**, 10046 (2005).

6. M. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, A. Lochtefeld, J. Appl. Phys. **97**, 011101 (2005).

7. G. Abstreiter, H. Brugger, T. Wolf, H. Jorke, H. J. Herzog, Phys. Rev. Lett. **54**, 2441 (1985).

8. U. König, A. J. Boers, F. Schäffler, E. Kasper, Elec. Lett. **28**, 160 (1992).

9. N. Søndergaard, Y. He, C. Fan, R. Han, T. Guhr, H. Q. Xu, J. Vac. Sci. Technol. B **27**, 827 (2009).

10. J. Grönqvist, N. Søndergaard, F. Boxberg, T. Guhr, S. Åberg, J. Appl. Phys. **106**, 053508 (2009).

11. V. Schmidt, P. C. McIntyre, U. Gösele, Phys. Rev. B **77**, 235302 (2008).

12. J. J. Wortman, R. A. Evans, J. Appl. Phys. **36**, 153 (1965).

13. Y. Sun, S. E. Thompson, T. Nishida, Strain effect in semiconductors: Theory and device applications (Springer, New York, 2010).

14. G. L. Bir, G. E. Pikus, Symmetry and strain-induced effects in semiconductors (Wiley, New York, 1974).

15. C. G. Van de Walle, Phys. Rev. B **39**, 1871 (1989).

16. M. M. Rieger, P. Vogl, Phys. Rev. B **48**, 14276 (1993).

17. C. Tserbak, H. M. Polatoglou, G. Theodorou, Phys. Rev. B **47**, 7104 (1993).

18. P. Friedel, M. S. Hybertsen, M. Schlüter, Phys. Rev. B **39**, 7974 (1989).

19. J. P. Morar, P. E. Batson, J. Tersoff, Phys. Rev. B **47**, 4107 (1993).

20. D. V. Lang, R. People, J. C. Bean, A. M. Sergent, Appl. Phys. Lett. **47**, 1333 (1985).

21. R. S. Wagner, W. C. Ellis, Appl. Phys. Lett. **4**, 89 (1964).

22. S. Nakashima, M. Hangyo, IEEE J. Quan. Elec. **25**, 965 (1989).

23. P. H. Tan, K. Brunner, D. Bougeard, G. Abstreiter, Phys. Rev. B **68**, 125302 (2003).

24. W. T. Masselink, Phys. Rev. Lett. **66**, 1513 (1991).

25. R. Dingle, H. L. Störmer, A. C. Gossard, W. Wiegmann, Appl. Phys. Lett. **33**, 665 (1978).

26. H. L. Störmer, A. Pinczuk, A. C. Gossard, W. Wiegmann, Appl. Phys. Lett. **38**, 691 (1981).

27. K. Ismail, M. Arafa, K. L. Saenger, J. O. Chu, B. S. Meyerson, Appl. Phys. Lett. **66**, 1077 (1995).

28. R. People, J. C. Bean, D. V. Lang, A. M. Sergent, H. L. Störmer, K. W. Wecht, Appl. Phys. Lett. **45**, 1231 (1984).

29. M. Arafa, P. Fay, K. Ismail, J. O. Chu, B. S. Meyerson, I. Adesida, IEEE Elect. Dev. Lett. **17**, 124 (1996).

30. U. König, F. Schäffler, IEEE Elect. Dev. Lett. **14**, 205 (1993).

31. K. M. Varahramyan, D. Ferrer, E. Tutuc, S. K. Banerjee, Appl. Phys. Lett. **95**, 033101 (2009).

32. J. Nah, K. M. Varahramyan, E.-S. Liu, S. K. Banerjee, E. Tutuc, Appl. Phys. Lett. **93**, 203108 (2008).

33. J. Nah, E-S Liu, K. M. Varahramyan, D. Shahrjerdi, S. K. Banerjee, E. Tutuc, IEEE Trans. on Elect. Dev. **57**, 491 (2010).

Vita

David Carl Dillen was born in North Tonawanda, New York on January 17, 1986, the second child of Daniel and Mary Ann Dillen. After graduating from Grand Island Senior High School in June 2004, he went on to study Electrical Engineering at Rensselaer Polytechnic Institute (RPI) in Troy, New York. During his time there, he was admitted to several engineering honor societies, including Tau Beta Pi and Eta Kappa Nu. He was also a four-year member of RPI's NCAA football team, where he was named as an "Academic All-American" by ESPN during his senior year. From the summer of 2007 to the spring of 2008, David worked as an undergraduate research assistant in the group of Professor E. Fred Schubert. In his time with the group, he focused mainly on the standardization of techniques used in the measurement of light-emitting-diode efficiency. In May of 2008, David graduated *summa cum laude* from RPI with a Bachelor of Science degree in Electrical and Computer Engineering. The following fall, he began his graduate studies in the Electrical Engineering department of the University of Texas at Austin, studying solid-state electronics. In April 2009, David joined the research group of Professor Emanuel Tutuc where he currently works with core-shell nanowire based electronic devices. After receiving his Master of Science degree in 2011, he intends to continue work towards a Ph.D. in Electrical Engineering at UT Austin.

Permanent email address: david.dillen@gmail.com

This thesis was typed by the author.